A 1.5mW, 200MHz CMOS VCO for Wireless Biotelemetry

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Abstract–Few people have studied the problem of physiological data transmission at the rates required by NASA's *Life Sciences-Advanced BioTelemetry System* (LS-ABTS). Implanted telemetry eliminates the problems associated with wire breaking the skin, and permits experiments with awake and unrestrained subjects. Our goal is to build a low-power 174-216MHz RF transmitter suitable for short range biosensor and implantable use. A system architecture based on a frequency-locked loop frequency synthesizer is presented, and a novel differential frequency discriminator that eliminates the need for a frequency divider is also proposed. The Hajimiri phase noise model was used to optimize the VCO for minimum power consumption. A test chip was fabricated in a 0.5μm, 3V CMOS process. Measured phase noise for a 1.5mW, 200MHz ring oscillator VCO is -80dBc/Hz at 100KHz offset, showing good agreement with the theory.

Currently, NASA-Ames Research Center is developing the Life Sciences-Advanced BioTelemetry System (LS-ABTS) to conduct space-based animal research [1]. *In vivo* experiments require anesthetized animals and hard-wired connections to the implant creating a risk of infection due to transcutaneous wires. Wire breakage, movement artifacts, ground loops and 60Hz pick-up can also cause problems. In collaboration with the Fetal Treatment Center at UCSF, NASA is also developing a system for wireless telemetry of physiological parameters of fetuses for monitoring and identifying distress after pre-natal surgery [2]. An implant that will monitor heart rate, temperature, pH, and amniotic fluid pressure is required to operate *in utero* for up to 3 months. A low-power highly integrated radio transmitter is key to the success of these projects.

The most important parameter of an implanted biotelemetry system is power dissipation. Power dissipation and implant lifetime determine the size of the battery which ultimately determines the size of the implant. A significant portion of the power budget for any implantable telemetry system is allocated to the generation of the RF carrier. Given this need for small, low-power wireless devices for biotelemetry, a low-power, integrated frequency synthesizer is required.

Traditionally, frequency synthesizers have been implemented using a phase-locked loop (PLL). Figure 1 shows the block diagram and power budget for a state-of-the-art CMOS PLL synthesizer used in microprocessor clock generation [3]. In a PLL synthesizer, the VCO frequency is divided and then compared to a reference frequency by a phase detector. The phase detector drives a low-pass filter that generate the control voltage for the VCO. The major sources of power dissipation are the VCO (73%) and the frequency divider (22%). To reduce power we have to address these blocks first.

We propose a frequency-locked loop (FLL) architecture (fig.2) that uses a differential frequency discriminator (DFD). In the past, quadricorrelators and rotational frequency detectors [4] have been used to aid the frequency acquisition process in a PLL, but have been superseded by simpler phase-frequency detectors with charge pumps [5].

The proposed FLL does not require a frequency divider, which represents 22% of the power budget for the PLL example just shown. The FLL can perform frequency comparison directly without a divider (N=1) by using a DFD implemented with switched capacitor circuits. In operation, current I_1 is generated by switches S_1, S_2 and capacitor C_1, and is inversely proportional to the reference frequency driving the switches, F_{REF}, and the value of C_1. Current I_2 is also inversely proportional to the feedback frequency, and the value of C_2. Current mirror M_1/M_2 force these two currents to be equal, resulting in the following relationship:

$$F_{OUT} = (C_1/C_2) \, F_{REF}$$

where the output frequency is determined solely by the capacitor ratio, C_1/C_2. A linear analysis using a single pole filter shows that this is a first order system, and thus inherently stable (neglecting sample-data effects).

A PLL tracks the phase noise of the reference signal, relaxing the close-in phase noise requirements of the VCO (provided that the reference has better phase noise than the VCO). However, a FLL tracks the VCO's frequency, not phase, forcing more stringent requirements on the VCO. The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required. In biotelemetry, data rates are low, and channel spacing wide, relaxing the phase noise requirements. This makes it feasible to use voltage-controlled ring oscillators which are easy to integrate and do not require any external components.

The VCO design is critical in the performance of the FLL synthesizer as the phase noise at the output of the FLL is solely a function of the phase noise of the VCO. The VCO consists of a 4-stage differential ring oscillator (fig.3). The differential buffers used (fig.4) have been shown to have excellent noise and power supply rejection characteristics [6]. Frequency control is achieved by changing the biasing of the buffer stages which determine the delay through each cell. The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases. The Hajimiri phase noise model [7] was used to optimize the VCO for minimum power dissipation. The single-sideband phase noise of a differential

ring oscillator in the $1/f^2$ region ($\Delta f > 136$KHz) can be approximated by

$$L\{\Delta w\} = 10 \log \{64kT/I_{DD}E_CL_{EFF}(fo^2/\Delta w^2)\} \text{ dBc/Hz}$$

where I_{DD} is the tail current of a single stage, E_C is the critical field, and L_{EFF} is the gate length of the differential-pair devices. Using this equation we plotted a series of phase noise curves for different values of I_{DD}. We selected the 100µA curve, for a total current drain of 500µA at 200MHz (3V supply).

A test chip was fabricated through MOSIS using the HP 0.5µm CMOS process. The VCO voltage-to-frequency transfer characteristic was measured and is shown in fig.6 for different supply voltages. Using an HP8590B Spectrum Analyzer, the phase noise was measured at -82dBc/Hz for 100KHz offset from a 200MHz carrier. Test results using a more accurate phase noise measurement test set are shown in figure 7 for operation at 150.9MHz, along with the theoretical phase noise performance predicted by the Hajimiri model. These measurements are within 2dB of the predicted values for frequency offsets between 10Hz and 1MHz.

A low-power biotelemeter suitable for chronic sensor implant studies is being developed. It implements a frequency synthesizer based on the FLL architecture just described. The FLL synthesizer does not require a frequency divider with its associated power dissipation, but it imposes more stringent phase noise requirements on the VCO. To minimize power consumption of the VCO, a design technique using the Hajimiri phase noise model was presented. Measurements of phase noise show good agreement with the theory.

References:

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[3] V. Kaenel, et al., "A 320MHz, 1.5mW at 1.35V CMOS PLL for Microprocessor Clock Generation", *Intl. Solid-State Circuits Conference*, Feb. 1996, pp.132-133.
[4] D. G. Messerschmitt, "Frequency Detector for PLL Acquisition in Timing Recovery", *IEEE Trans. Comm.*, vol. COM-27, Sep. 1979, pp. 1288-95.
[5] F. M. Gardner, "Charge Pump Phase-Lock Loops", *IEEE Trans. Comm.*, vol. COM-28, Nov. 1980, pp. 1849-1858,
[6] M. Horowitz, et al. , "PLL Design for a 500MB/s Interface", *Intl. Solid-State Circuits Conference*, Feb. 1993, pp.160-161.
[7] A. Hajimiri, T.H. Lee, "A General theory of phase noise in electrical oscillators", *IEEE Journal of Solid-State Circuits*, to be published in 1997.
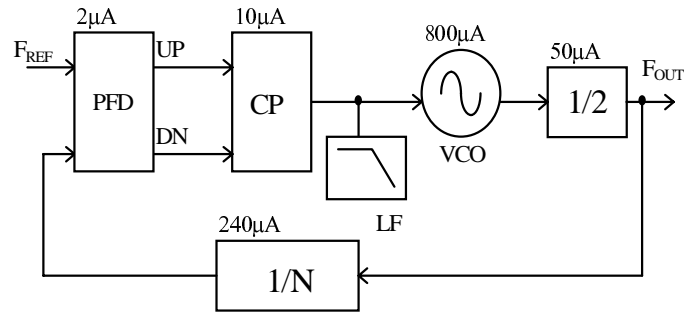
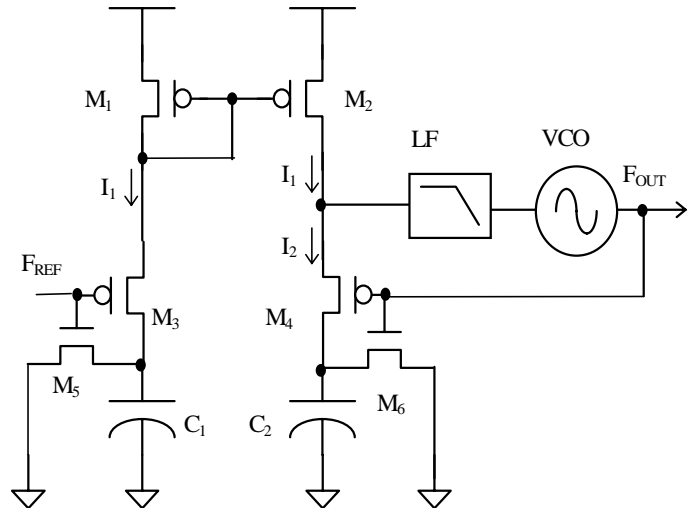**Figure 1. Typical PLL frequency synthesizer power budget**
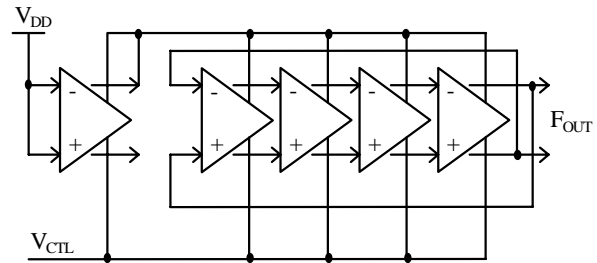

Figure 2. Frequency-locked loop frequency synthesizer

Figure 3. Differential ring oscillator VCO
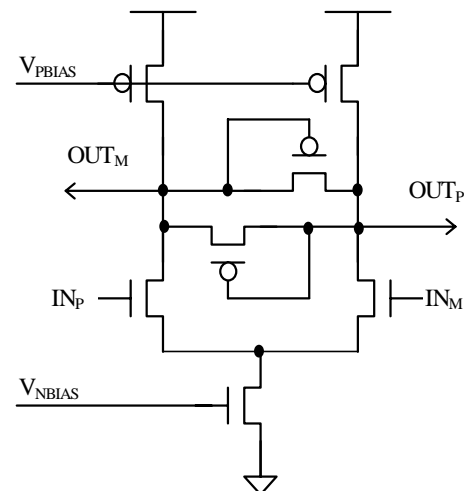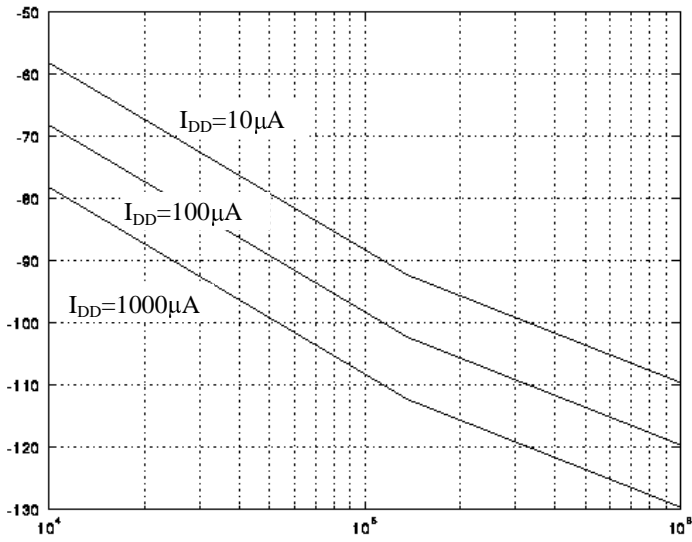

Figure 4. Differential delay buffer cell

Figure 5. Single-sideband phase noise (dBc/Hz) for differential ring oscillator at 200MHz

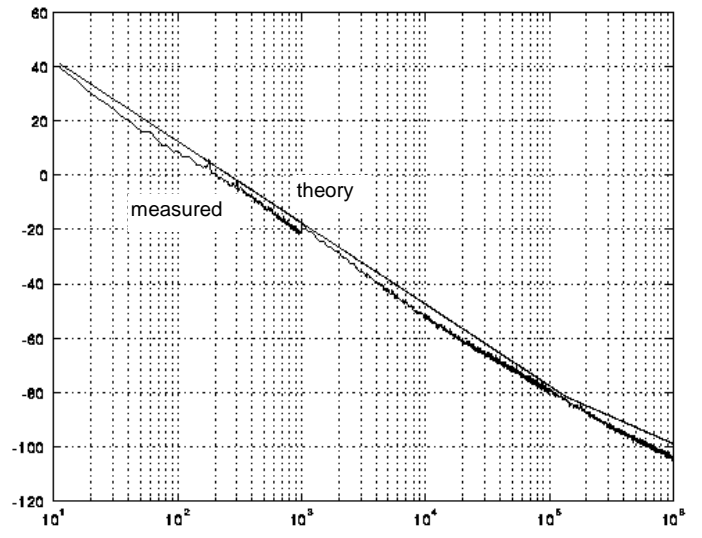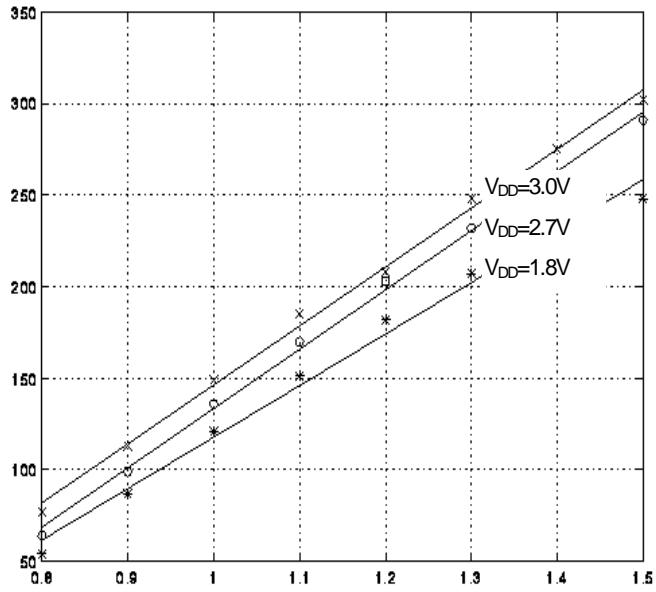**Figure 7. Phase noise (dBc/Hz) test results at 150.9MHz**

Figure 6. VCO frequency (MHz) vs. control voltage