A Low Power Frequency Synthesizer for Wireless Biotelemetry

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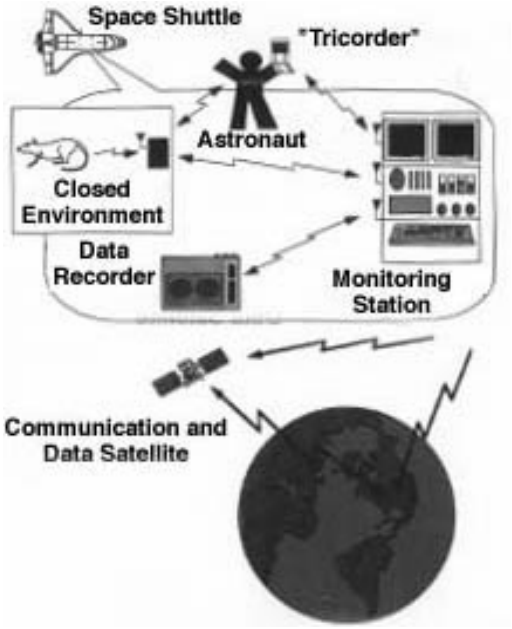
Outline

- ***Introduction***
- Frequency Synthesizer Design
- Phase Noise Theory
- Voltage-controlled Oscillator Design
- Simulation and Measured Results
- Conclusion and Acknowledgements

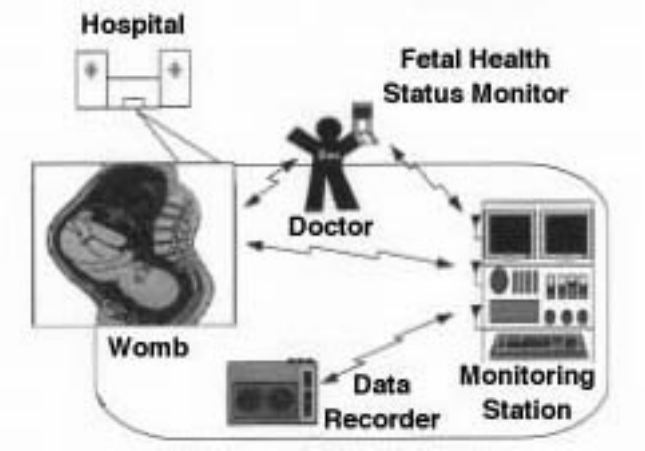
Biotelemetry is Crucial for Space Life Sciences

- On the ground, animals can be housed separately for data collection, and tethered systems are feasible. In space, where volume is very costly, animals must be group-housed, making tethers undesirable.
- *In vivo* experiments often require anesthetized animals and hard-wired connections to the implant, creating a risk of infection due to transcutaneous leads.



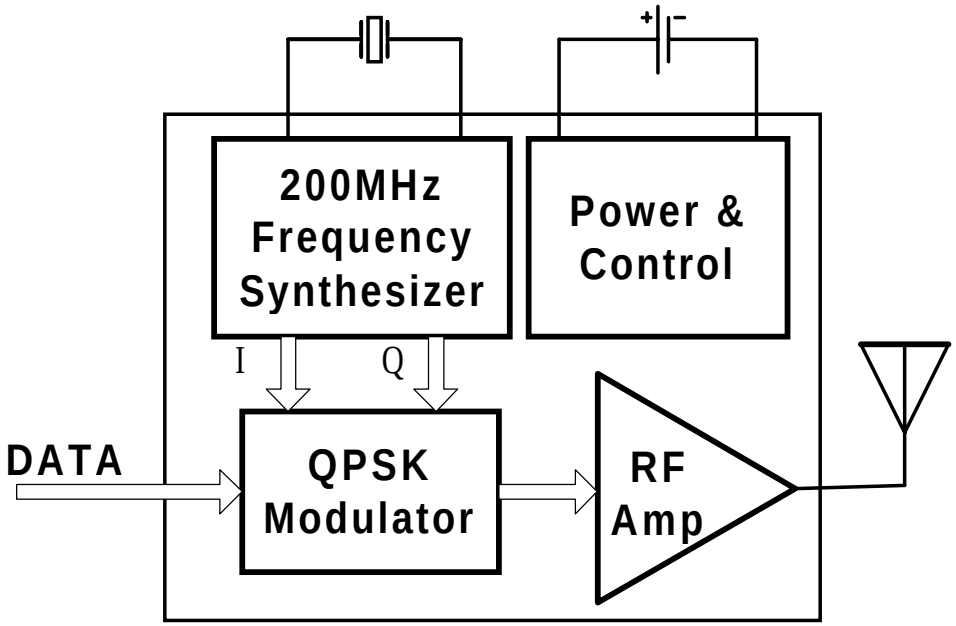
- **NASA-Ames Research Center** is developing the Advanced BioTelemetry System (ABTS) to conduct space-based animal research.
- Implantable biotelemetry supports real-time data gathering. It allows experiments with awake and unrestrained animals, and eliminates problems with lead breakage, movement artifacts, and ground loops.
- **NASA** needs a low power implantable transmitter that can relay biosensor data using the 174-216MHz band.

Human Applications for Biotelemetry



- **NASA** researchers are collaborating with doctors at the **University of California-San Francisco's (UCSF) Fetal Treatment Center** to adapt space biosensor and biotelemetry technology for the monitoring of fetuses with life-threatening congenital conditions.
- At **UCSF's Fetal Treatment Center** there is a need for telemetry of physiological parameters of human fetuses for monitoring and identifying distress after surgery.
- A telemetry implant that will monitor heart rate, temperature, pH, and amniotic fluid pressure is required to operate *in utero* for up to 3 months.

Goal: An Implantable Biotelemetry Transmitter



- Frequency: 174-216MHz
- Data Rate: 100 kbps
- Modulation: Quadrature Phase Shift Keying (QPSK)
- Range: 1 meter
- Power source: 3.6 V, 750mAH lithium
- Implant lifetime: 100 hours (continuous)
- Implant volume: 5 cm^3 (including battery)

- **Our goal is to design and build a low-power radio transmitter in CMOS suitable for short range biosensor and implantable use.**

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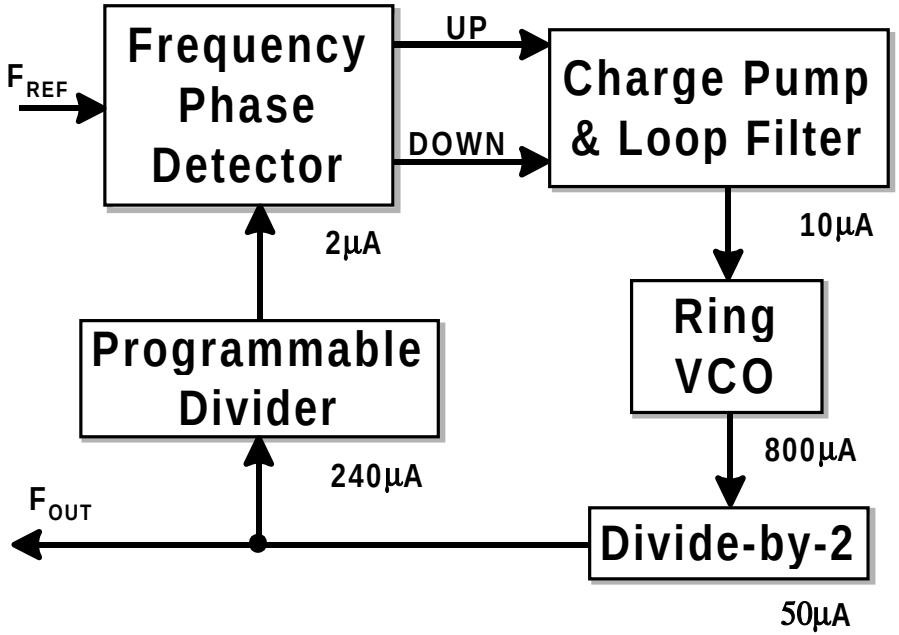
Phase-locked Loop Frequency Synthesizer

- The most important parameter of an implanted biotelemetry system is power dissipation.
- A significant portion of the power budget is allocated to the generation of the RF carrier.
- Traditionally, frequency synthesizers have been implemented using phase-locked loops (PLLs).
- The major sources of power dissipation are the VCO (73%) and the frequency divider (22%).

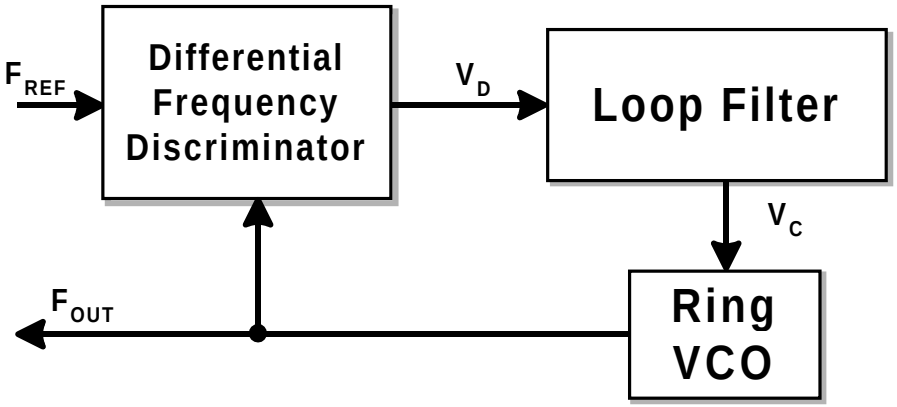


Power budget for a typical CMOS PLL frequency synthesizer used in microprocessor clock generation[1].

[1]V. Kaenel, et al., "A 320MHz, 1.5mW at 1.35V CMOS PLL for Microprocessor Clock Generation", *Intl. Solid-State Circuits Conference*, Feb. 1996, pp.132-133.

Frequency-locked Loop Frequency Synthesizer

$$V_D(s) = K_D \cdot (F_{REF} - F_{OUT})$$



$$LF(s) = \frac{1}{sC}$$

$$F_{OUT}(s) = K_V \cdot V_C(s)$$

- Closed loop response:

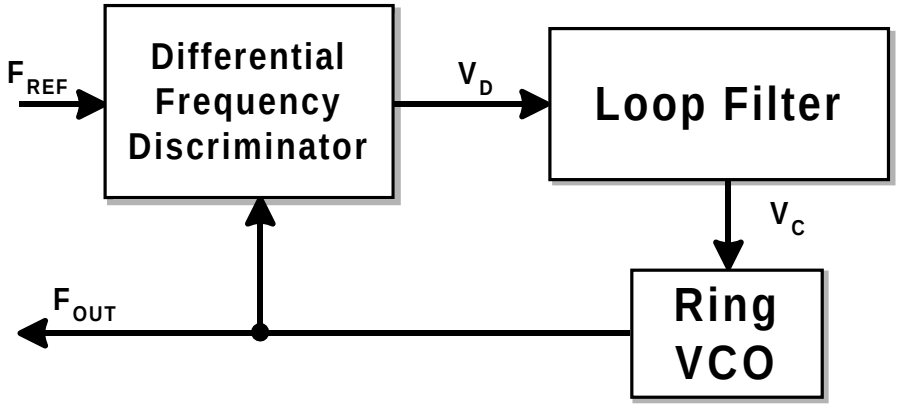
$$\frac{F_{OUT}}{F_{REF}}(s) = \frac{1}{1 + s/\omega_N}$$

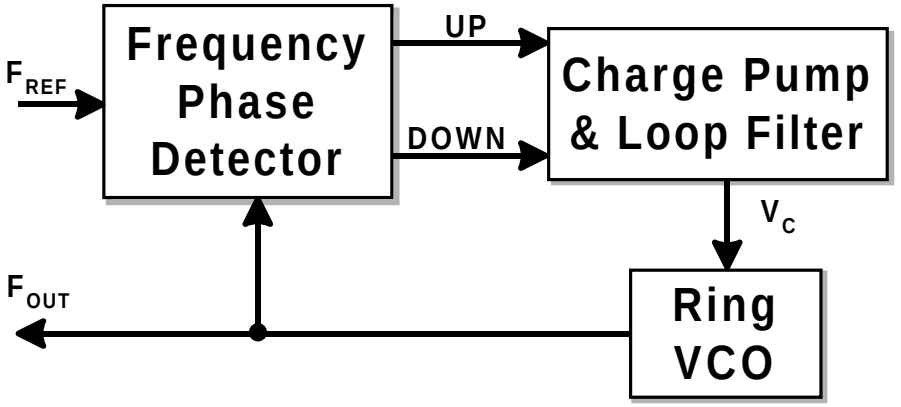
- where ω_N (rad/s) is the loop bandwidth

$$\omega_N = \frac{K_V \cdot K_D}{C}$$

- A linear analysis using a single pole filter shows that this is a first order system, and thus inherently stable (neglecting sampled-data effects).

FLL vs. PLL Frequency Synthesizers



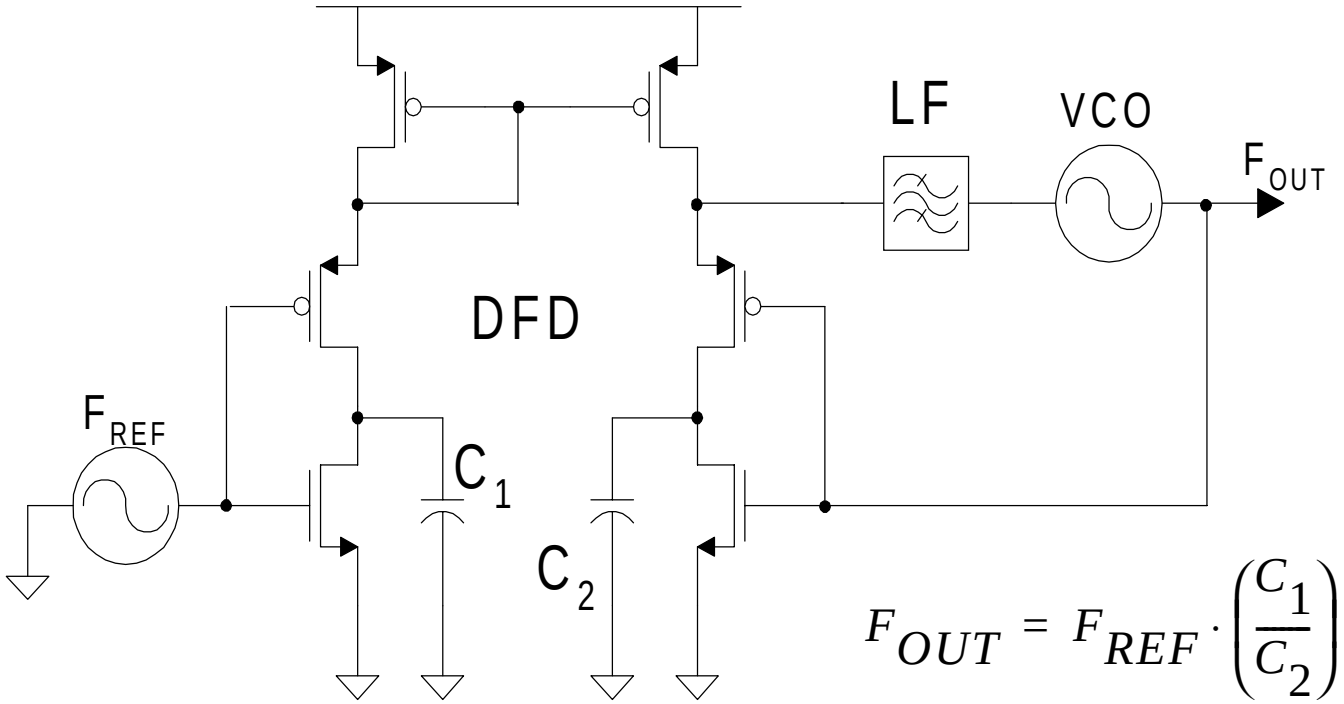


$$\frac{F_{OUT}}{F_{REF}}(s) = \frac{1}{1 + s/\omega_N}$$

$$\frac{\Theta_{OUT}}{\Theta_{REF}}(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

- The controlled variable in a FLL is frequency not phase.

Differential Frequency Discriminator



- This FLL does not require a frequency divider, which represents 22% of the power budget for the PLL example just shown.
- The FLL can perform frequency comparison directly without a divider by using a DFD implemented with switched capacitor circuits.
- The output frequency is determined by the capacitor ratio, C_1/C_2, and the reference frequency.

Power Dissipation vs. Phase Noise

- In a synthesizer application, the reference frequency source is usually a crystal oscillator with very low phase noise.
- A PLL tracks the phase noise of the reference signal, relaxing the close-in phase noise requirements of the VCO.
- However, a FLL tracks the VCO's frequency, not phase, forcing more stringent requirements on the VCO.
- The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required.
- In biotelemetry, data rates are low (10-100kbps), and channel spacing wide (3MHz), relaxing the phase noise requirements for the VCO.

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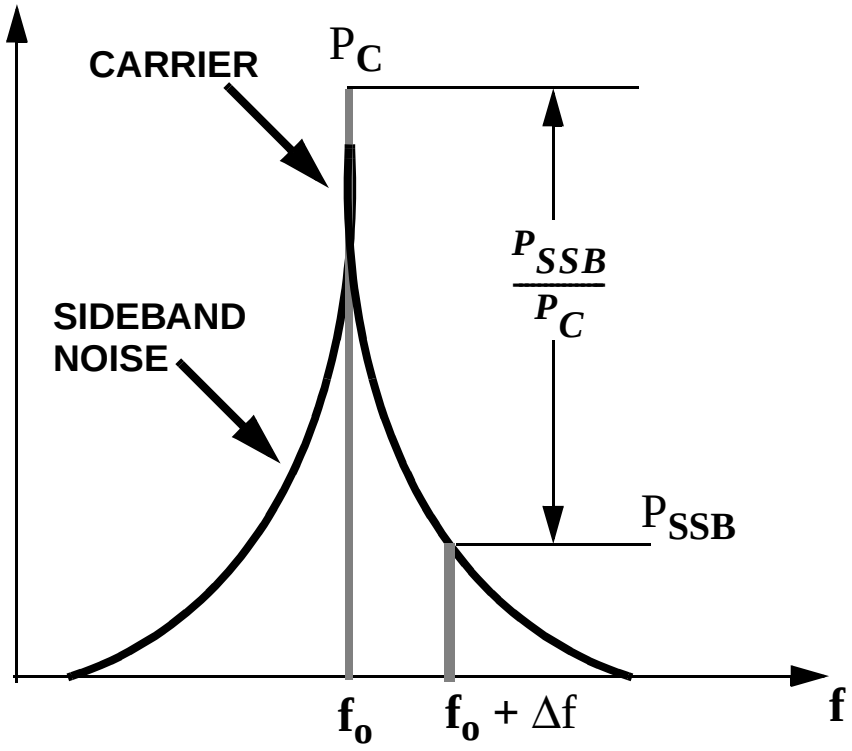
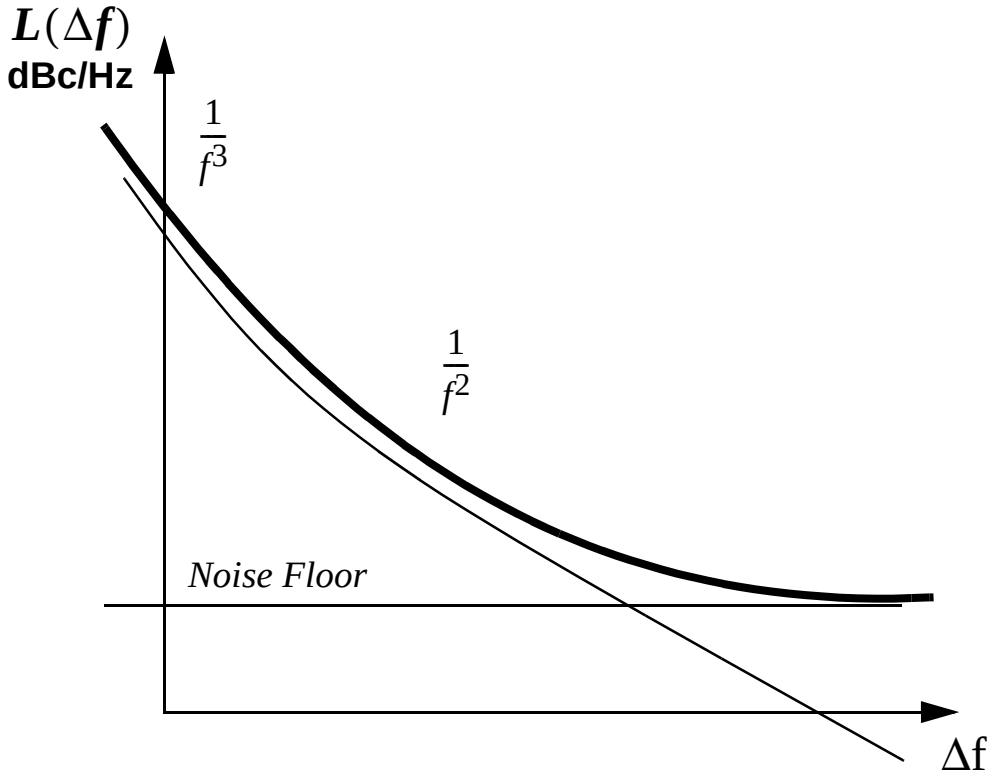
What is Phase Noise?

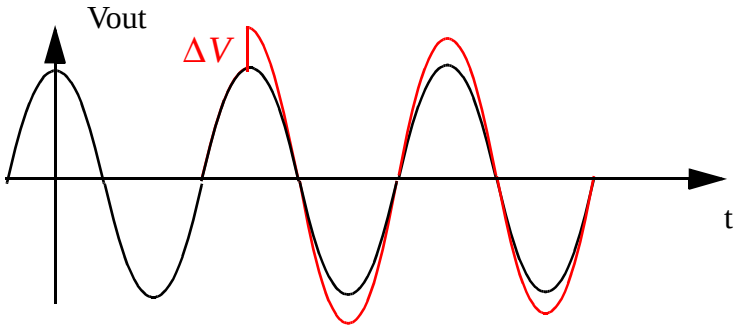




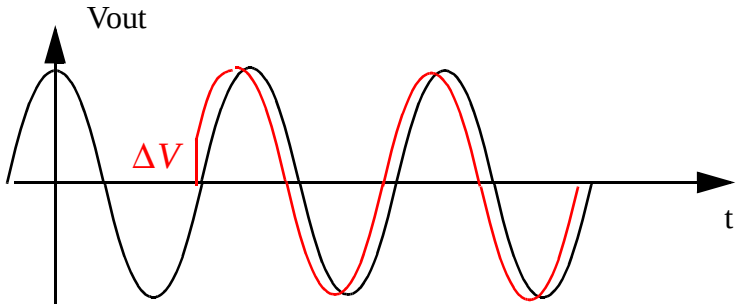
- The output power of an oscillator is not concentrated exclusively at the carrier frequency alone.
- The spectral distribution on either side of the carrier is known as spectral sidebands.

- Phase noise power is represented as a ratio of power in 1Hz bandwidth in one sideband to the power of the carrier.
- This ratio is specified in units of dBc/Hz at some frequency offset from the carrier.

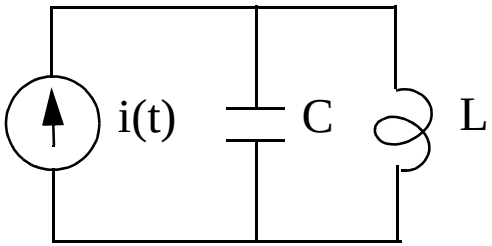
Oscillators are Time-Variant Systems



- A current impulse injected at the peak only changes the amplitude and has no effect on the phase.



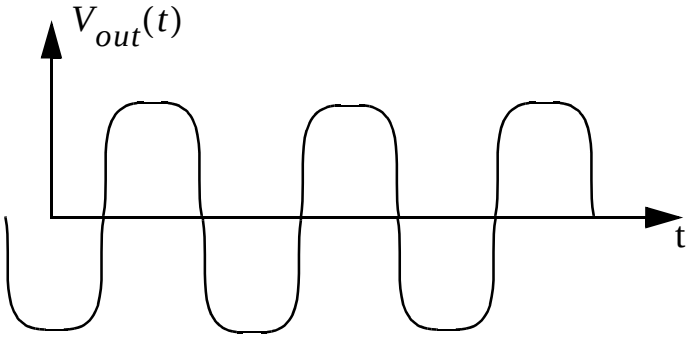
- A current impulse injected at the zero-crossing only changes the phase and has minimal effect on the amplitude.

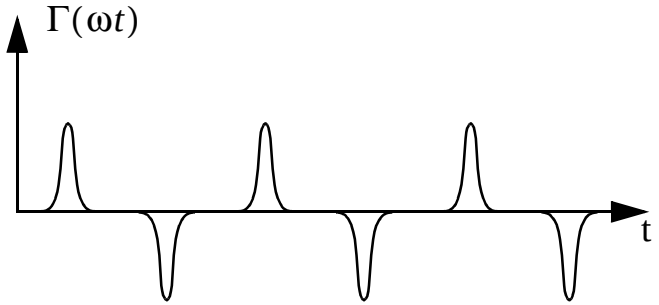


$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau)$$

- where the Impulse Sensitivity Function $\Gamma(x)$ is a periodic function.
- and q_{max} is the maximum charge displacement in the tank.

Impulse Sensitivity Function for Ring Oscillators



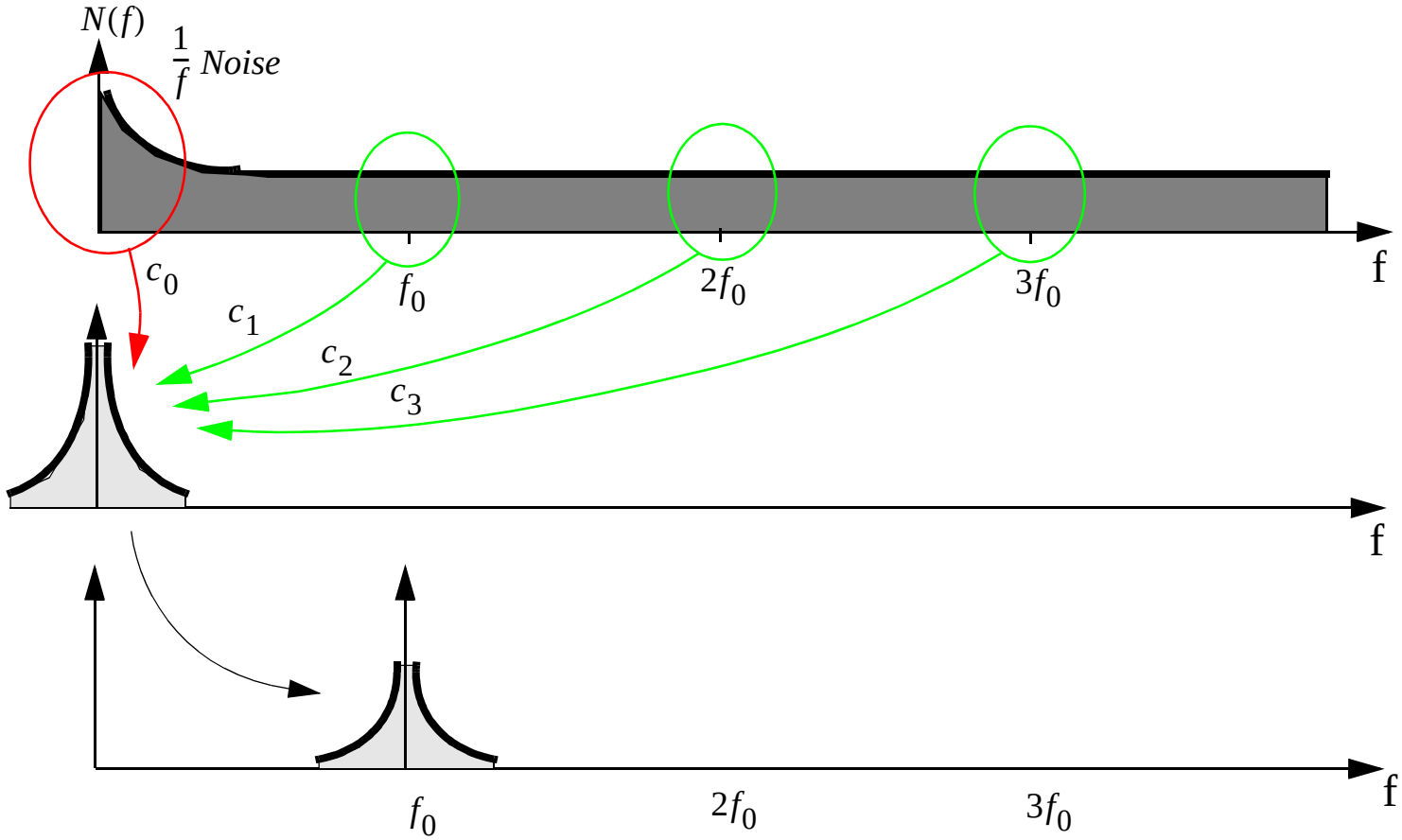


$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau)\cos(n\omega\tau)d\tau\right]$$

- $\Gamma(x)$ can be calculated directly from the waveform.
- Since $\Gamma(x)$ is periodic, it may be expressed as a Fourier series, and used in a superposition integral to determine the phase noise spectrum resulting from known device and circuit noise[1].

[1] T. Lee, "CMOS RF: No Longer an Oxymoron", *IEEE GaAs IC Symp.*, Oct. 1997, pp.244-247.

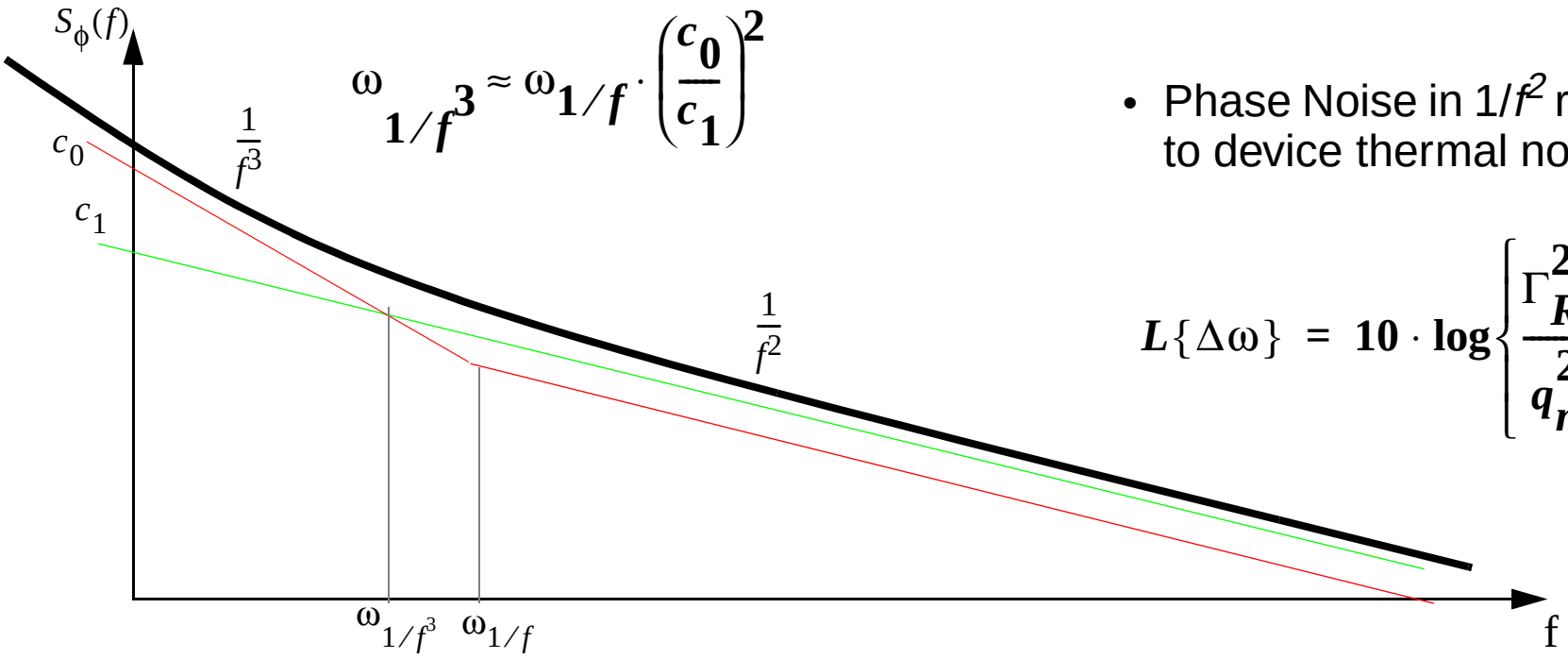
Upconversion of Device 1/f Noise



- Phase noise close to the carrier results from the folding of device noise centered at integer multiples of the carrier frequency.
- The upconversion of device 1/*f* noise occurs through c_0, the DC value of the ISF.
- The DC value of the ISF is governed by the symmetry properties of the waveform.

Hajimiri Phase Noise Model[2]

- Phase Noise in $1/f^3$ region is due to device $1/f$ noise.
- It is commonly assumed that the $1/f^3$ corner of phase noise is the same as the 1/f corner of the device noise spectrum.This is NOT the case.



$$\omega_{1/f^3} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2$$

- Phase Noise in $1/f^2$ region is due to device thermal noise.

$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{\Gamma_{RMS}^2}{q_{max}^2} \cdot \frac{i_n^2/\Delta f}{4\Delta\omega^2}\right\}$$

[2]A. Hajimiri, T. Lee, "A General Theory of Phase Noise in Oscillators", *IEEE Journal of Solid-State Circuits (in press).*

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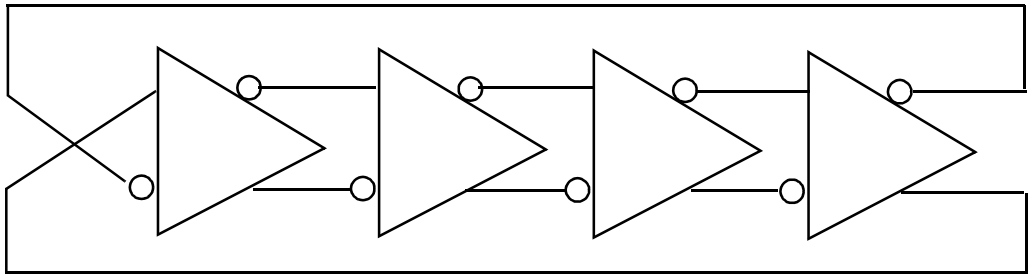
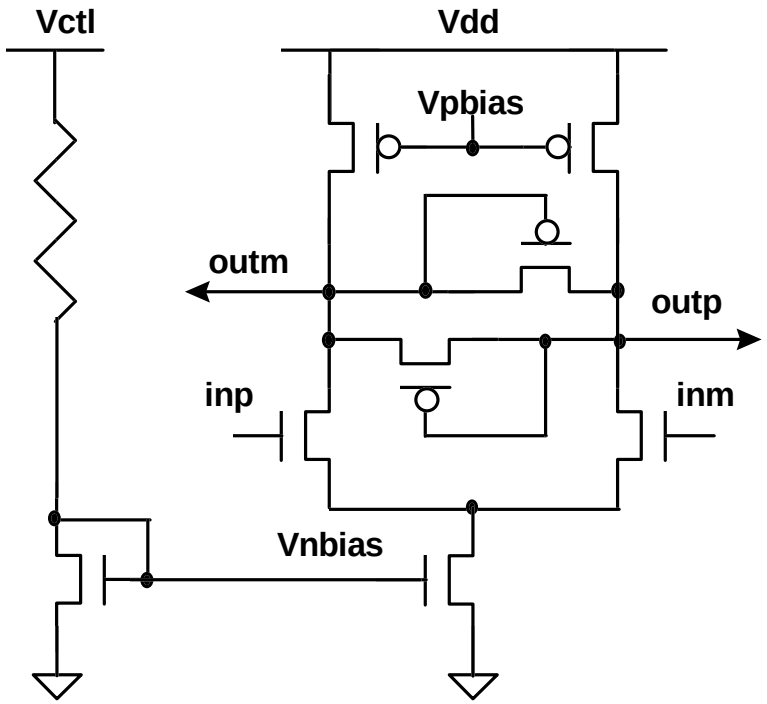
Voltage-controlled Oscillator Design

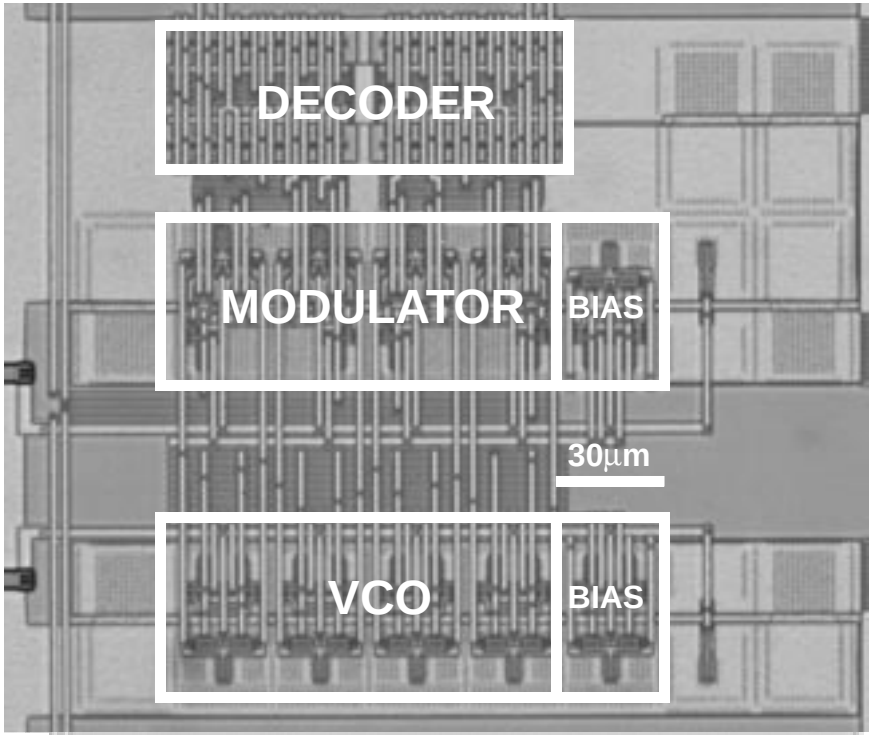


- The VCO design is critical in the performance of the FLL synthesizer as the phase noise at the output of the FLL is solely a function of the phase noise of the VCO.
- The VCO consists of a 4-stage differential ring oscillator[3].
- Frequency control is achieved by changing the biasing of the buffer stages which determines the delay through each cell.

[3] A.W. Buchwald, K.W.Martin, "High Speed Voltage Controlled Oscillators with Quadrature Outputs", *Electronics Letters*, 14 Feb. 1991, Vol. 27 No. 4, pp.309-310.

Differential Delay Buffer Design





- The differential buffers used have been shown to have excellent noise and power supply rejection characteristics[4].
- The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases.

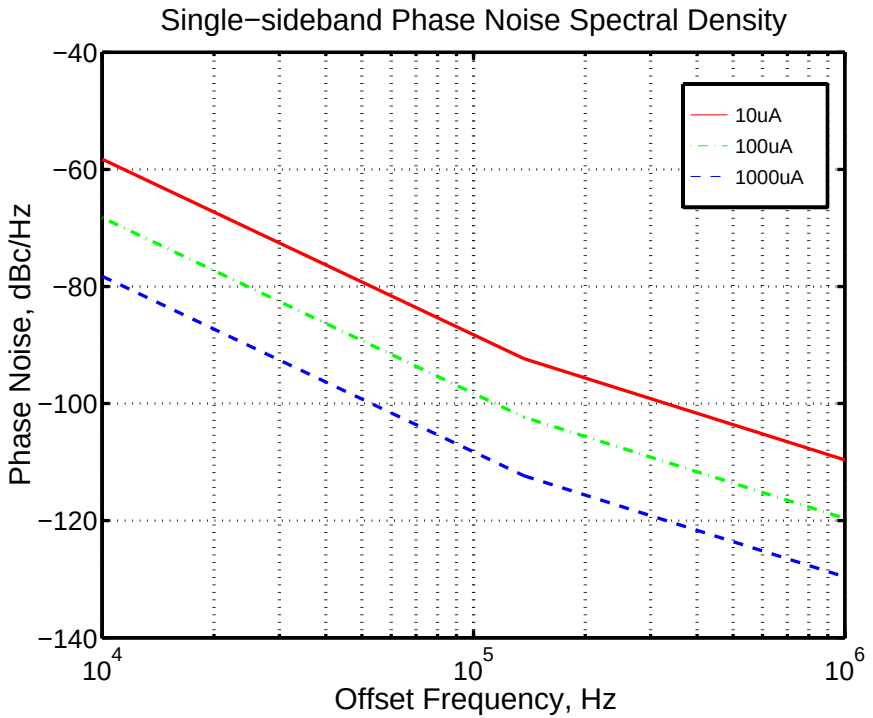
[4] M. Horowitz, et al., "PLL Design for a 500MB/s Interface", *Intl. Solid-State Circuits Conference*, Feb. 1993, pp.160-161.

Phase Noise Analysis of Ring Oscillator VCO

$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{64kT}{I_{DD}{}^{E}C^{L}EFF}\left(\frac{f_o{}^{2}}{\Delta\omega^{2}}\right)\right\}$$

Single-sideband phase noise (dBc/Hz) for a differential ring oscillator in the $1/f^2$ region

- I_{DD} is the tail current of a single stage
- E_C is the critical field (e.g., 4.918 V/µm)
- L_{EFF} is the gate length of the differential-pair devices (e.g., 0.5µm)
- We selected the 100µA curve, for a total current drain of 500µA at 200MHz.



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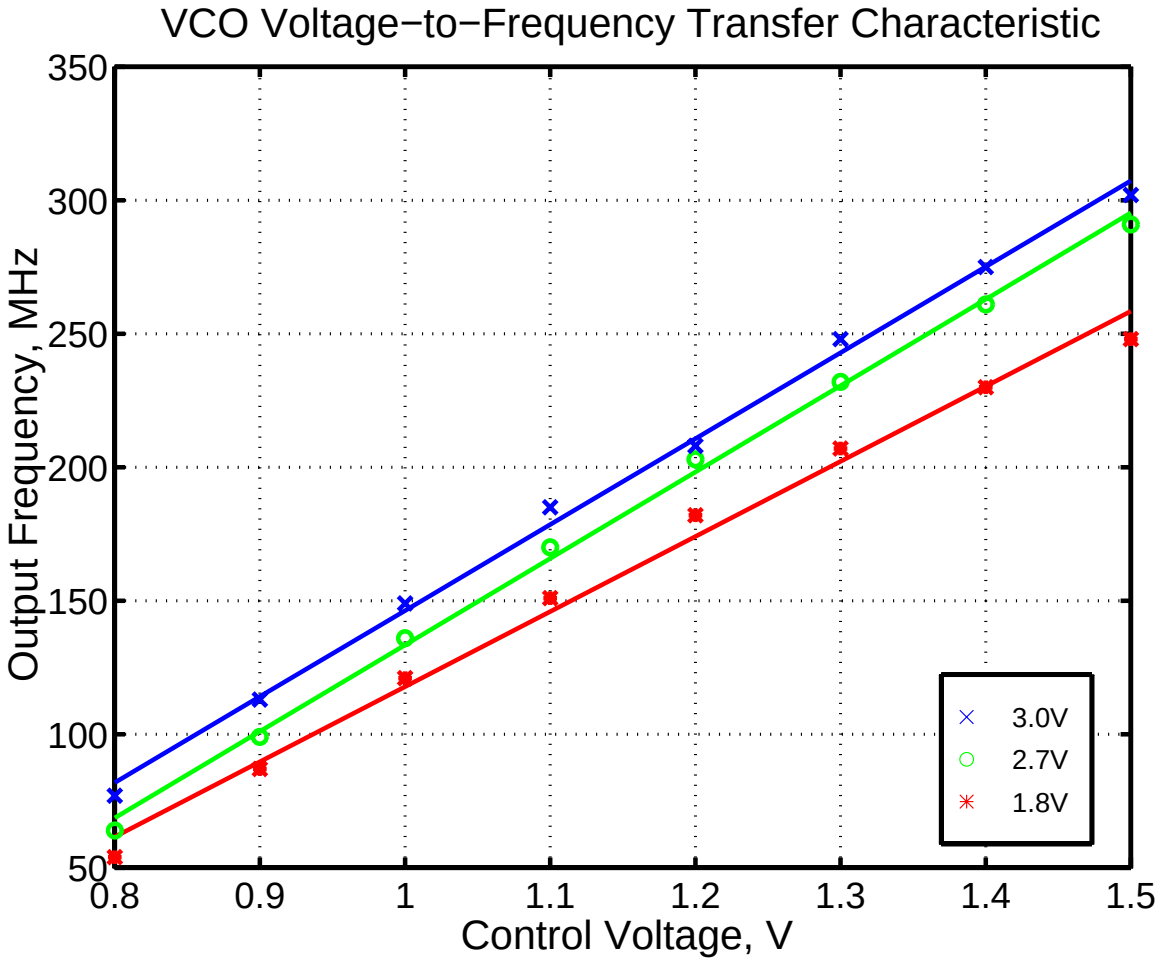
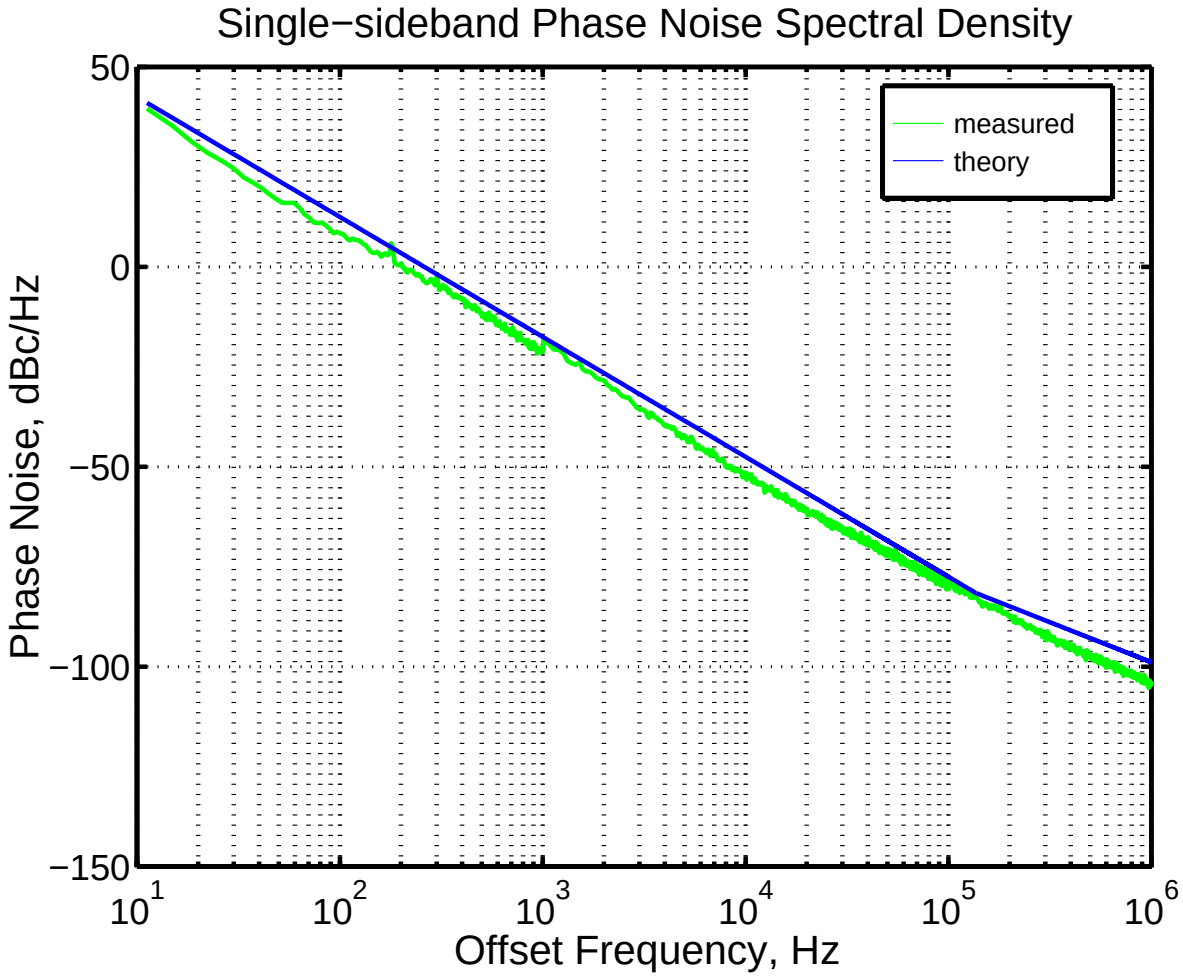
Test Results: VCO Transfer Characteristic



- Fabricated through MOSIS using the HP 0.5µm CMOS process.
- The VCO voltage-to-frequency transfer characteristic was measured for different supply voltages.
- Tuning Range: 350kHz-707MHz @3V
- VCO Gain = 321MHz/V @3V

Test Results: Phase Noise



- Using an HP8590B spectrum analyzer, the phase noise was measured at -82dBc/Hz for 100kHz offset from a 200MHz carrier.
- These measurements are within 2dB of the predicted values for frequency offsets between 10Hz and 1MHz.

Test results using RDI's NTS-1000A phase noise measurement test set, along with the theoretical phase noise performance predicted by the Hajimiri model (f_c=150.9MHz).

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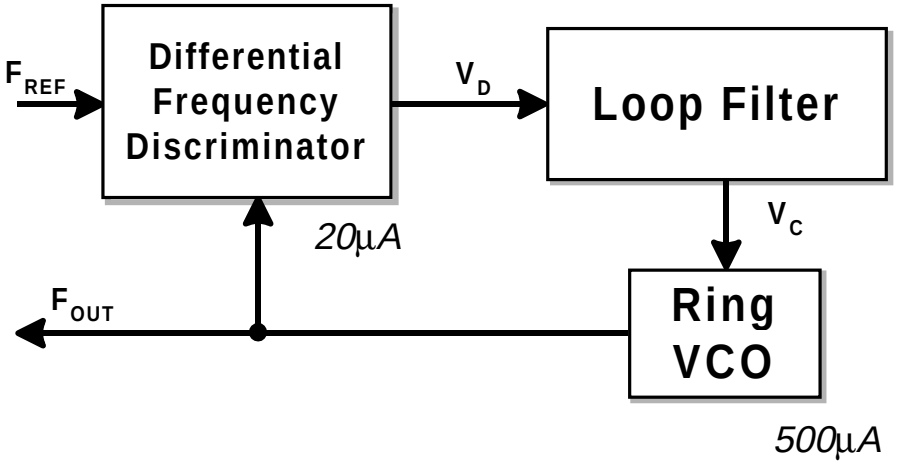
Conclusions



- The frequency-locked loop (FLL) synthesizer imposes more stringent phase noise requirements on the VCO.
- A design technique using the Hajimiri phase noise model was presented.
- A 200MHz ring oscillator VCO was designed and fabricated in 0.5µm CMOS.
- Measurements of phase noise show good agreement with the theory.

Acknowledgements

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