CMOS Injection-locked Ring Oscillator Frequency Dividers

March 29, 2001

Rafael J. Betancourt-Zamora
Stanford Microwave Integrated Circuits Laboratory
Paul G. Allen Center for Integrated Systems
Department of Electrical Engineering
Stanford University
http://www-smirc.stanford.edu/

Outline

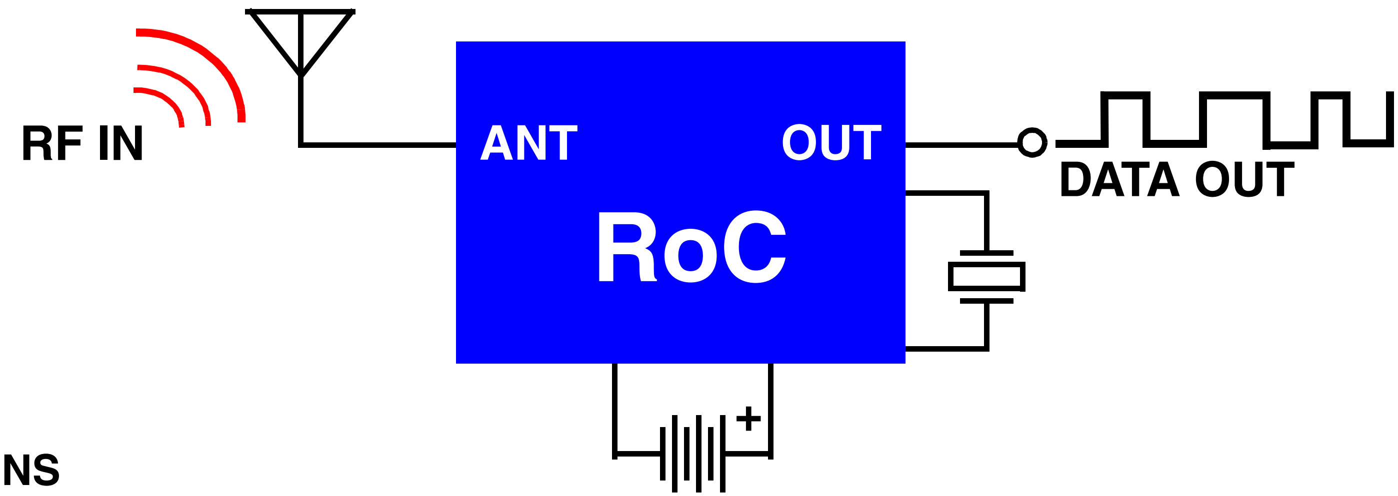
- ***Goals***
- Ring Oscillator Overview
- Injection Locking Theory
- Circuit Implementation
- Measured Results
- Conclusion

Goals

- Appreciate the trade-offs of low-power frequency synthesis
- Understand the operation of Ring Oscillators
- Understand the Injection-locking mechanism
- Grasp the limitations of Injection-locked Frequency Dividers
- Design Injection-locked Frequency Divider using a Ring Oscillator

Motivation

A short-haul, low-power, radio-on-a-chip (RoC) that requires no external components can enable novel applications that are not economically feasible otherwise.



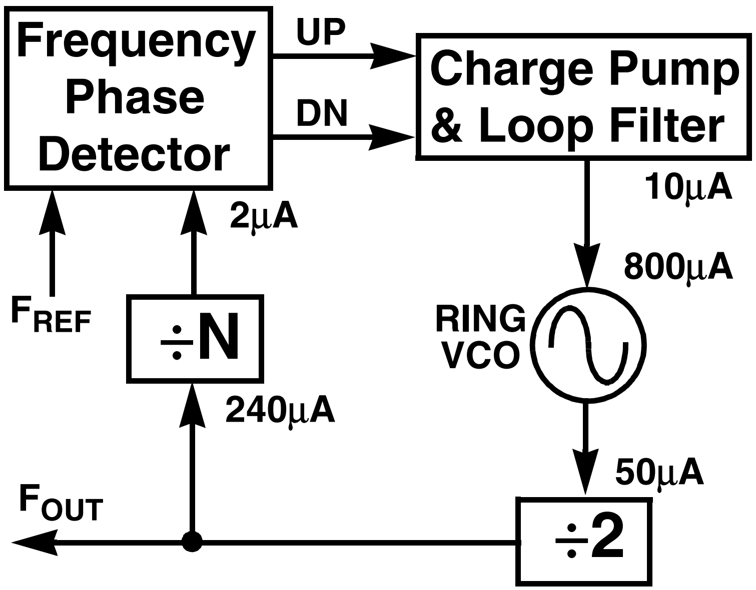
APPLICATIONS

- Ambulatory health monitoring and biotelemetry
- Building and environmental monitoring
- Distribution and retail inventory management
- Wireless Internet access
- Home and factory automation

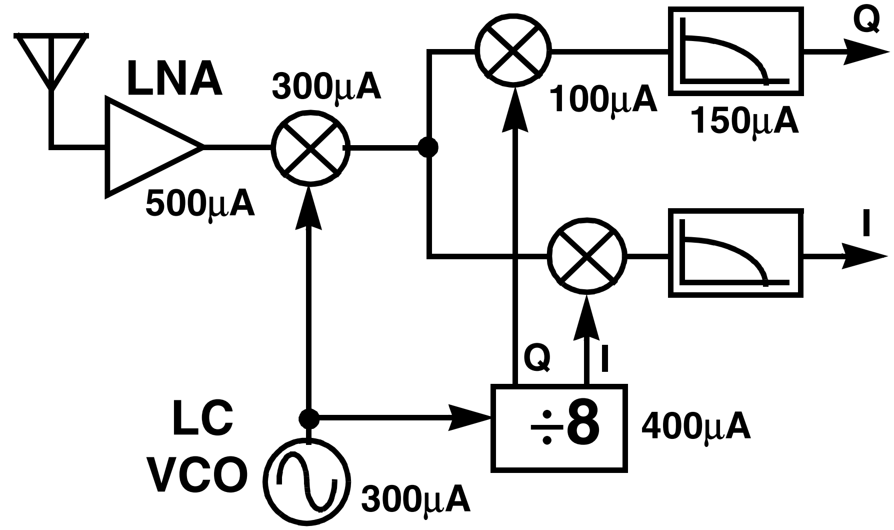
ISSUES

- A significant portion of the power budget is allocated to the generation of the RF local oscillator.
- Requires a low-power, completely integrated frequency synthesizer.

Low-power Frequency Synthesis



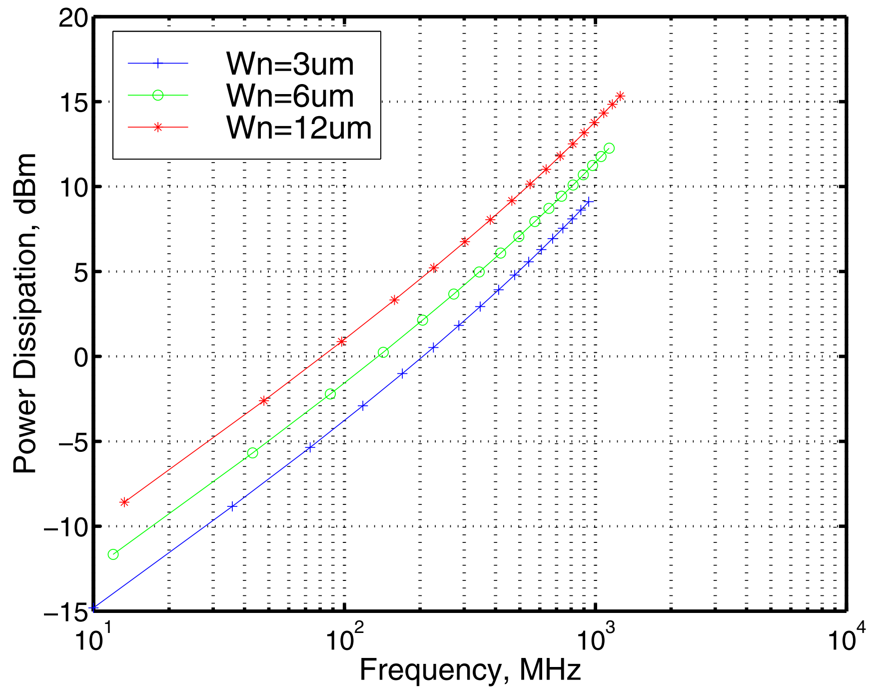
320 MHz CMOS PLL [V.Kaenel'96]

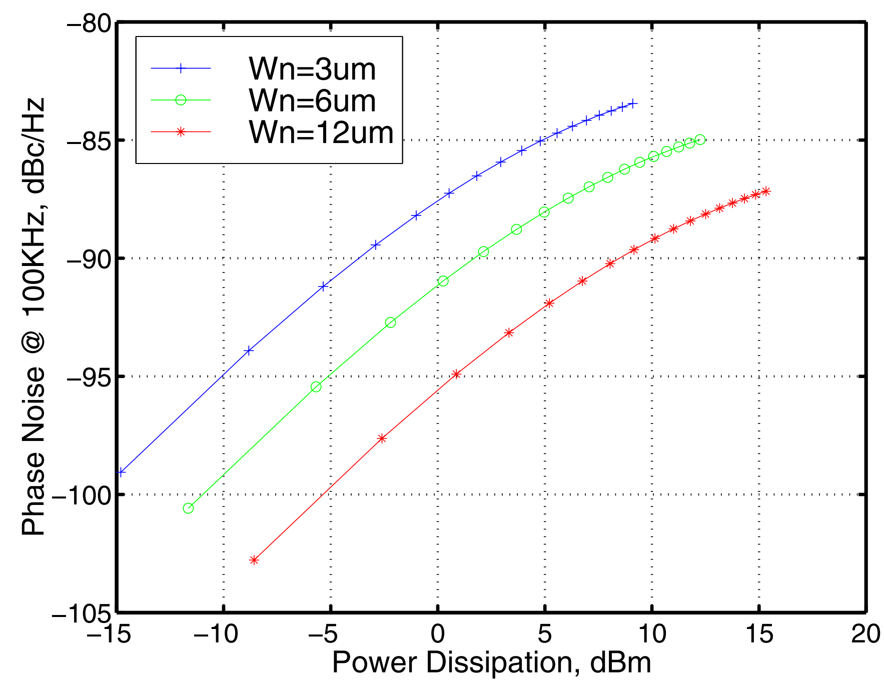


900 MHz CMOS RECEIVER [Darabi'00]

- Frequency synthesizers are implemented using Phase-locked Loops (PLLs).
- Major sources of power dissipation are the Voltage-controlled Oscillator (VCO) and the Frequency Divider.

Voltage-controlled Oscillator Trade-offs

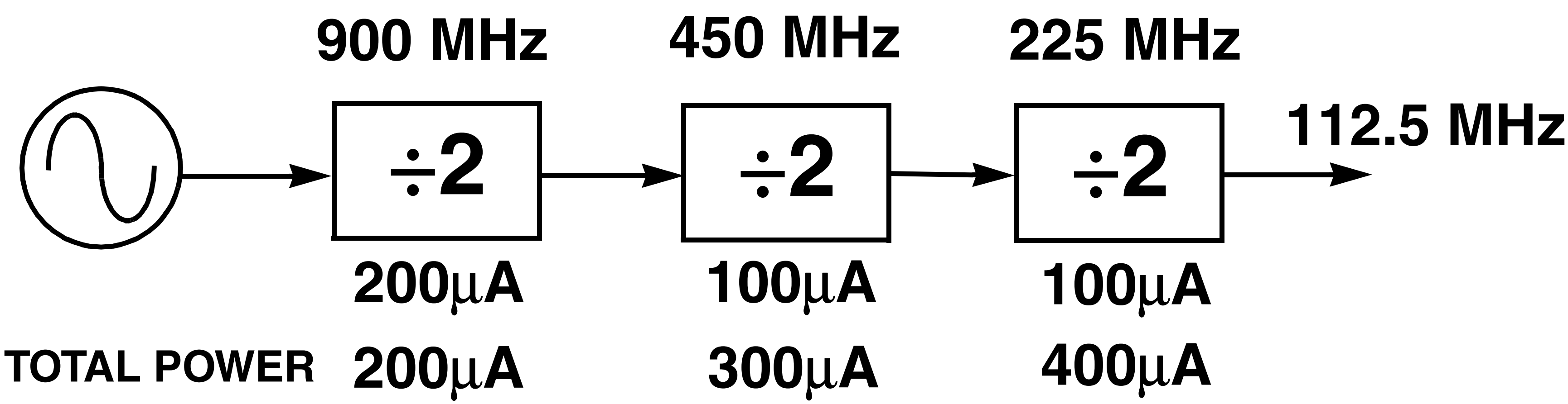




- The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required.
- A PLL tracks phase noise of the reference within its loop bandwidth, relaxing the close-in phase noise requirements of the VCO.

Frequency Divider Trade-offs

POWER INCREASES WITH DIVISION RATIO



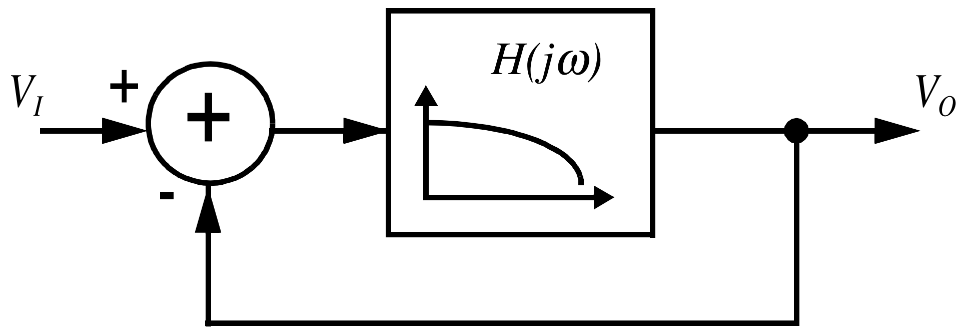
- Better understanding of low-power techniques for frequency division is essential to reduce the overall power dissipation of integrated frequency synthesizers.
- We propose a technique in which power ***decreases*** with division ratio. Are you interested?

Outline

- Goals
- ***Ring Oscillator Overview***
- Injection Locking Theory
- Circuit Implementation
- Measured Results
- Conclusion

How can a circuit oscillate?

- **BADLY-DESIGNED FEEDBACK AMPLIFIER**



Closed-loop Gain

$$A_V(j\omega) = \frac{H(j\omega)}{1 + H(j\omega)}$$

IF $H(j\omega_O) = -1$ **THEN** $\lim_{\omega \to \omega_o} A_V(j\omega) = \infty$

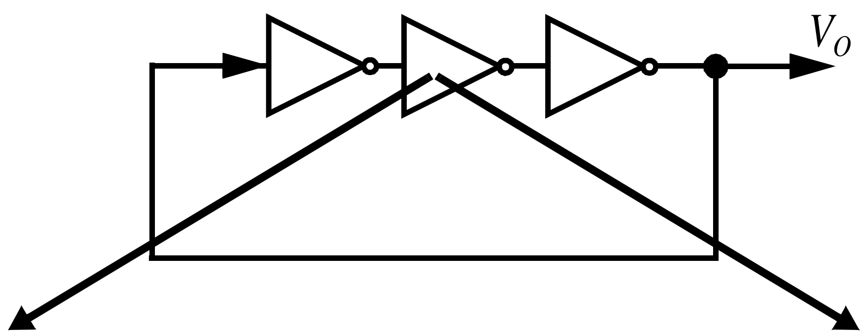
BARKHAUSEN CRITERIA

- Necessary conditions for oscillation
- Total phase shift around the loop is 360º
- Amplifies its own noise at ω_0
- Positive feedback or "regeneration"

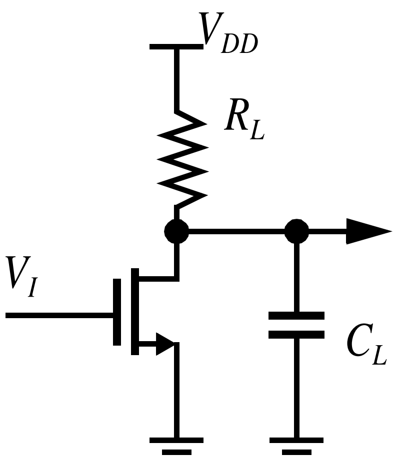
$$|H(j\omega_O)| \geq 1$$
$$\angle H(j\omega_O) = 180^{\circ}$$

What is a Ring Oscillator?

- **A RING OSCILLATOR CONSISTS OF A NUMBER OF GAIN STAGES IN A FEEDBACK LOOP**



SINGLE-ENDED



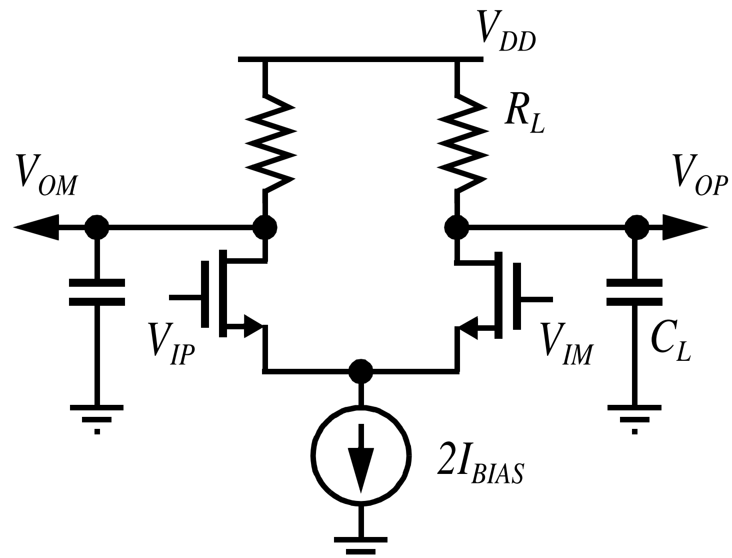
$$H_S(j\omega) = \frac{H_O}{1 + j\omega/\omega_P}$$

$$H_O = -g_m R_L \qquad \omega_P = \frac{1}{R_L C_L}$$

$$C_L = C_{GS} + (2 + g_m R_L) C_{GD} + C_{DB}$$

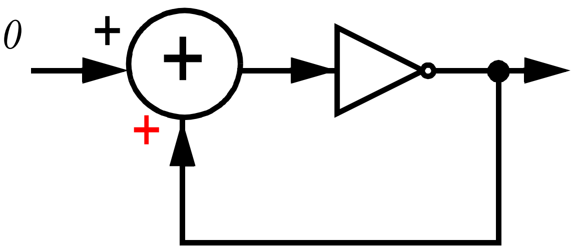
- Neglect feedforward zero $+g_m/C_{GD}$

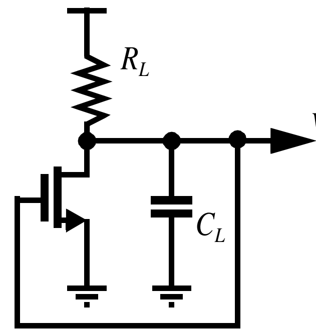
DIFFERENTIAL



Evolution of the Ring Oscillator

1 STAGE



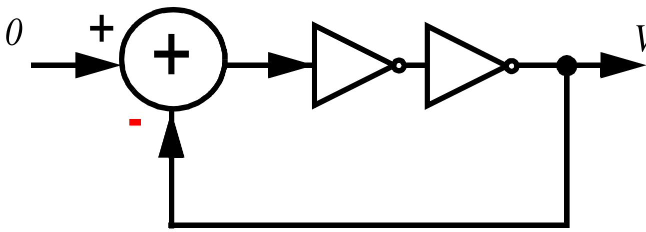


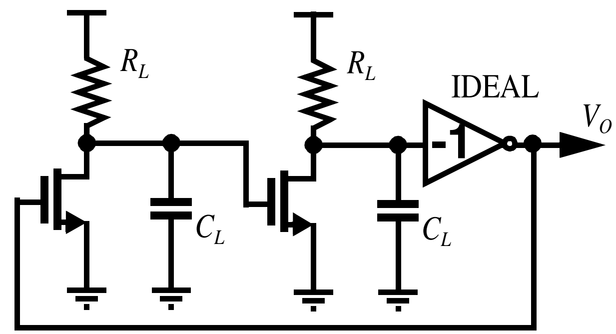
$$H(j\omega) = \frac{H_O}{1 + j\omega/\omega_P}$$

$$\angle H(j\omega)\big|_{\infty} = 90^{\circ}$$

INSUFFICIENT PHASE

2 STAGES



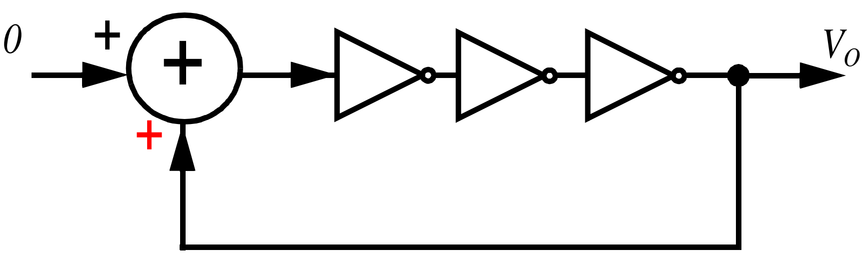


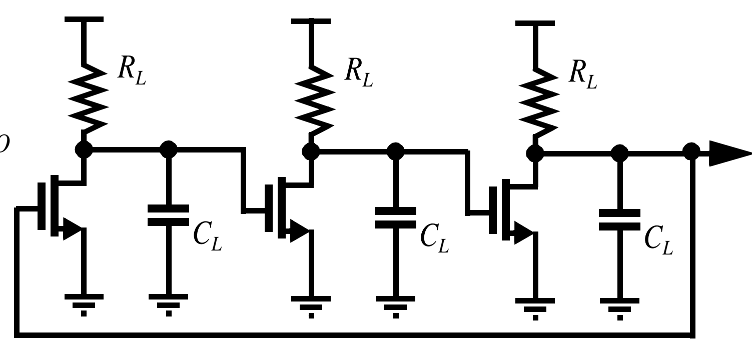
$$H(j\omega) = \frac{H_O^2}{(1 + j\omega/\omega_P)^2}$$

$$\angle H(j\omega)\big|_{\infty} = 180^{\circ}$$

INSUFFICIENT GAIN

3 STAGES



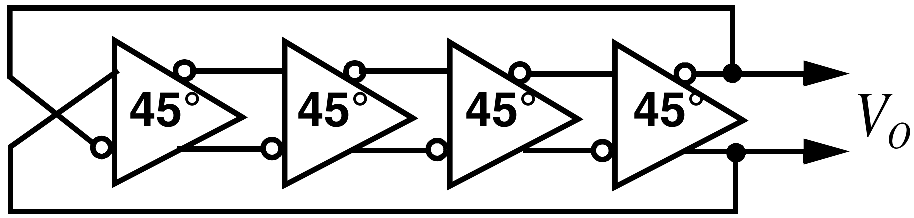


$$\angle H(j\omega)\big|_{\infty} = 270^{\circ}$$

IT WORKS!

Evolution of the Ring Oscillator (II)

4-STAGE DIFFERENTIAL RING OSCILLATOR



- EACH STAGE CONTRIBUTES 45° @ ω_O
- EACH POLE CONTRIBUTES 45° @ ω_P
- THUS $\omega_O = \omega_P$

IN GENERAL

$$H(j\omega) = \frac{H_O^n}{(1 + j\omega/\omega_P)^n}$$

PHASE CONDITION

$$\angle H(j\omega_o) = n \cdot \operatorname{atan}\left(\frac{\omega_o}{\omega_P}\right) = \pi$$

GAIN CONDITION

$$H_O \geq \sqrt{1 + \tan\left(\frac{\pi}{n}\right)^2}$$

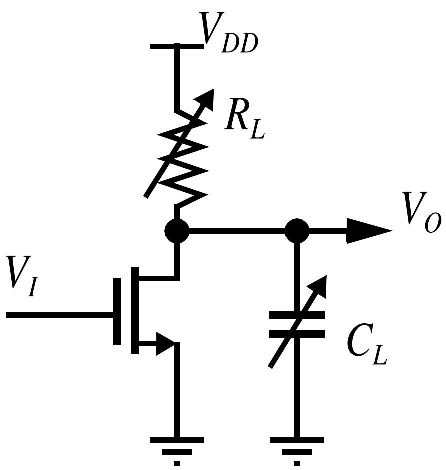
$$H(j\omega) = \frac{H_O^n}{\left(1 + j\frac{\omega}{\omega_o}\tan\left(\frac{\pi}{n}\right)\right)^n}$$

$$n > 2$$

LARGE SWING (AMPLITUDE LIMITED)

$$f_{osc} = \frac{1}{2nT_D} < f_o$$ **WHERE** $T_D \propto \tau_P$

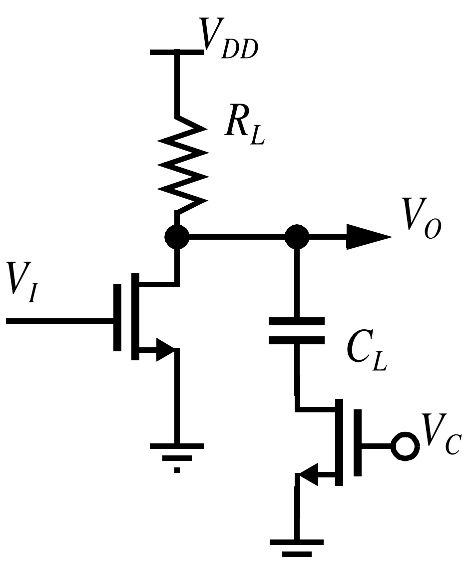
Voltage-Controlled Ring Oscillator



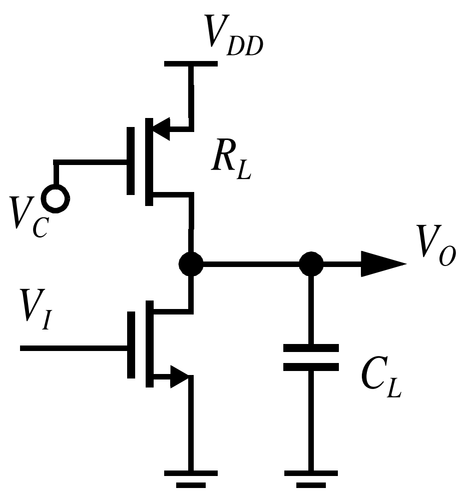
- Delay of each stage T_D is tuned by control input.
- Change delay by varying capacitance or resistance at each stage.

$$T_D \propto R_L C_L \qquad \omega_P = \frac{1}{R_L C_L}$$

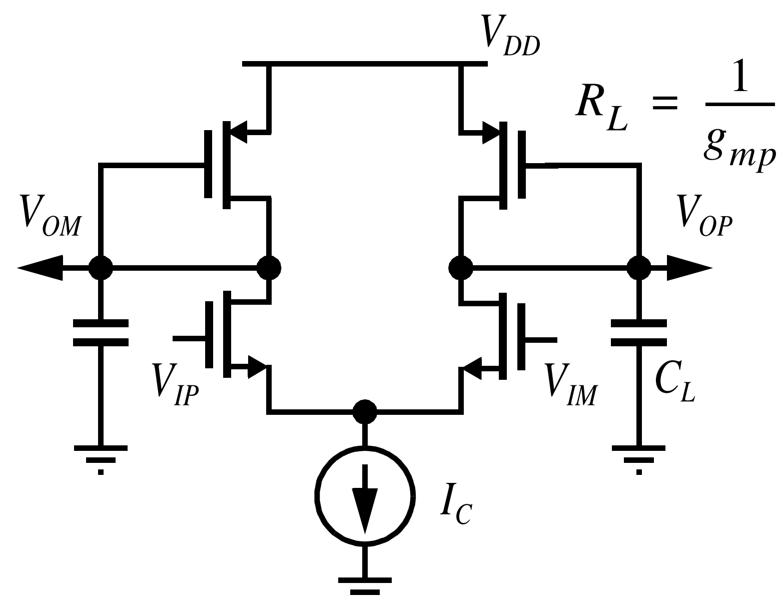
CAPACITIVE TUNING



TRIODE LOAD

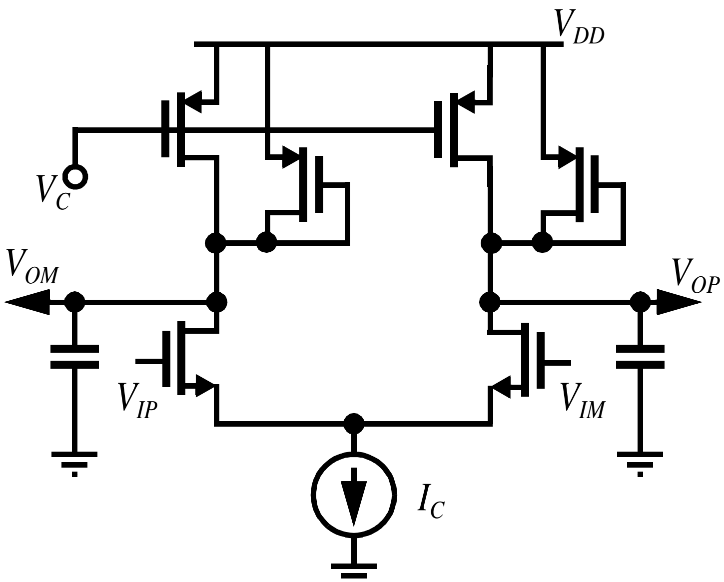


DIODE-CONNECTED LOAD

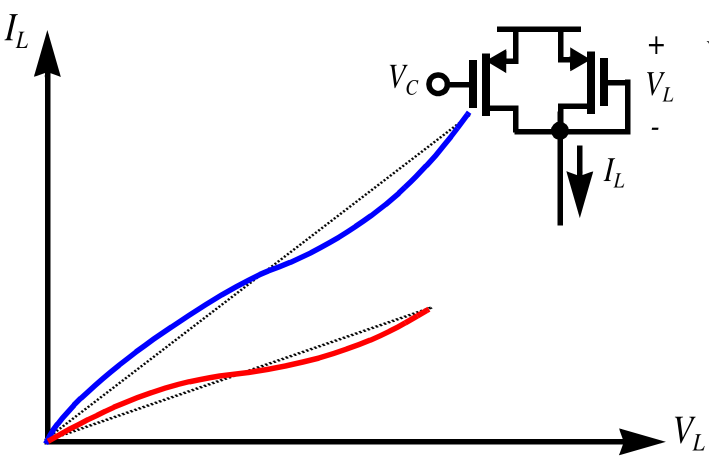


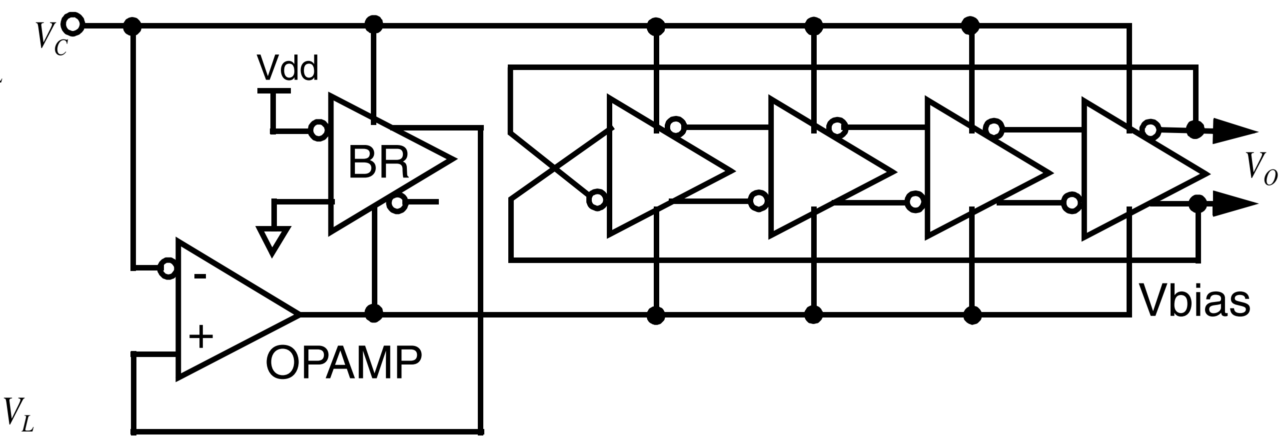
Voltage-Controlled Ring Oscillator (II)

SYMMETRIC LOAD [MANEATIS'94]



- Use buffers with replica-feedback biasing.
- V_C changes the bias I_C of the buffers.
- Replica bias ensures load symmetry by forcing the maximum single-ended swing $V_S = V_{dd} - V_C$
- Good supply noise rejection



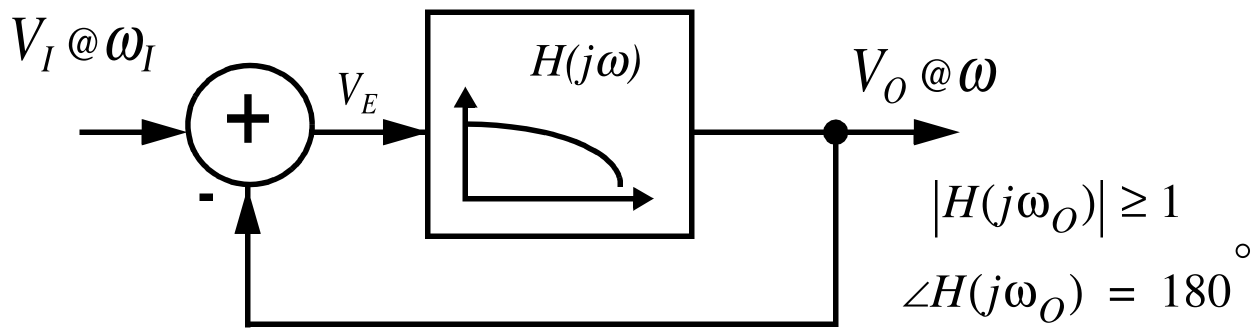


Outline

- Goals
- Ring Oscillator Overview
- ***Injection Locking Theory***
- Circuit Implementation
- Measured Results
- Conclusion

What is Injection Locking? [Adler 1946]

OSCILLATOR OUTPUT SYNCHRONIZES TO INJECTED SIGNAL



ASSUME $\omega_I \approx \omega_O$

$V_I << V_O$

Fast Amplitude Limiting Mechanism

- **IF** $V_I = 0$ **THEN** $\omega = \omega_O$
- **IF** $V_I \neq 0$ **THEN** ω shifts from free-running frequency, ω_O.
- Frequency shift is proportional to V_I / V_O.

Locking Range of Injection-locked Oscillator

$$\left|\frac{\Delta\omega_O}{\omega_O}\right| < \frac{V_I}{V_O} \cdot \frac{2}{n \sin\left(\frac{2\pi}{n}\right)}$$

$$\Delta\omega_O = \omega_O - \omega_I$$

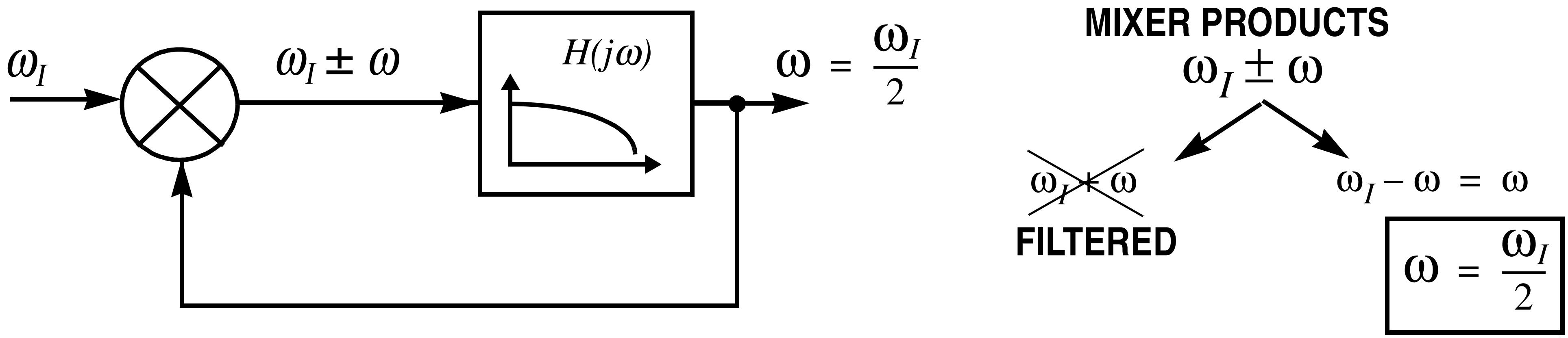
- Proportional to V_I/V_O.
- Inversely proportional to number of stages, *n*.
- Only valid for $V_I << V_O$

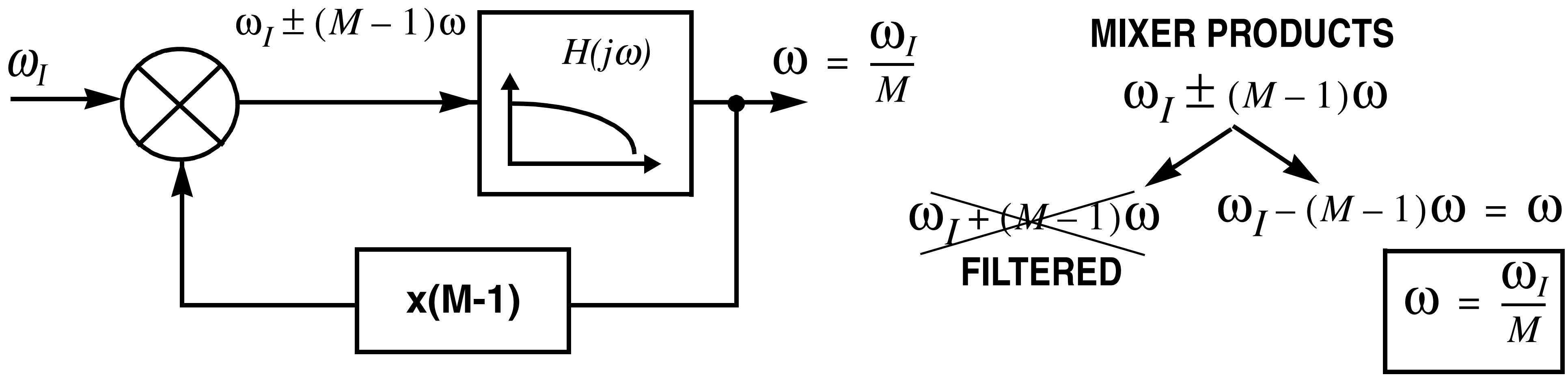
Superharmonic Injection Locking

- An oscillator can be injection-locked to a harmonic of the free-running oscillation frequency.
- This principle is used by all regenerative frequency dividers.
- Regenerative dividers are commonly used in applications where the frequency of operation is very high, beyond what can be achieved with flip-flop based circuits.
- Efforts at frequencies beyond 5 GHz have been reported using injection-locking to implement divide-by-2 prescalers in CMOS, and Si-BJT technologies.
- Commonly used at mm-wave frequencies in GaAs and SiGe

We want to exploit injection locking to achieve low-power frequency division.

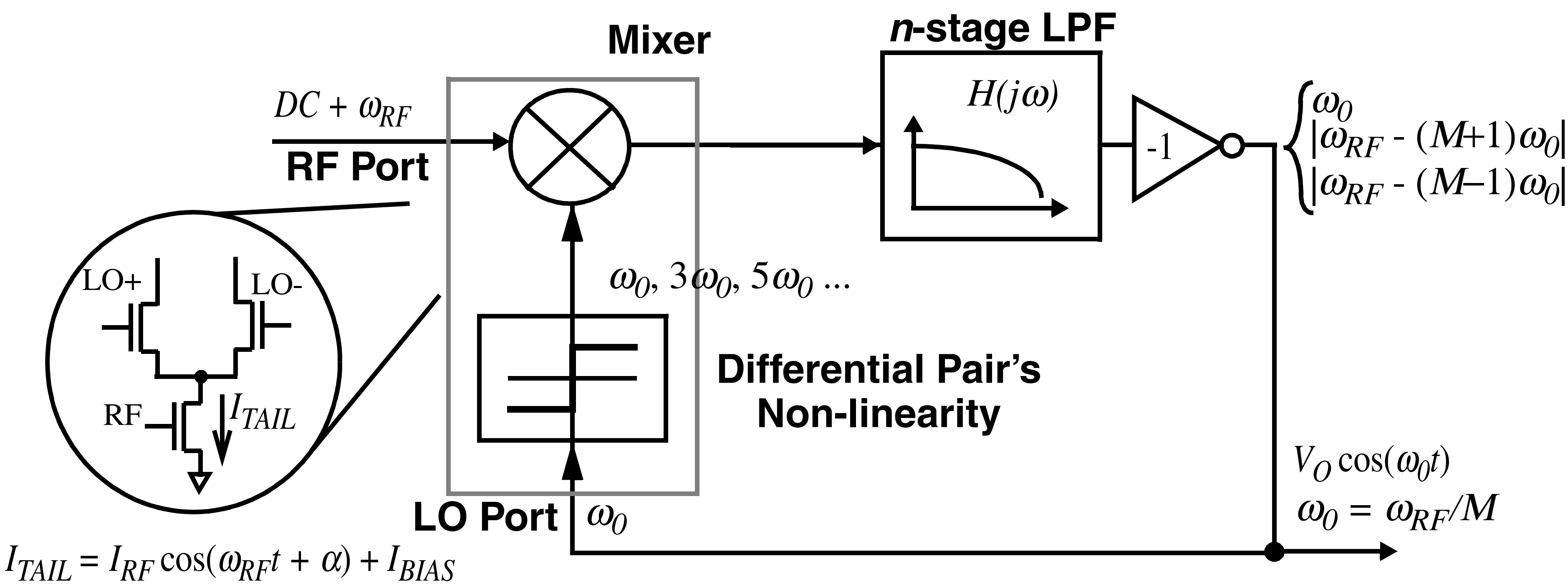
Regenerative Divider [Miller 1939]





- Can achieve division ratios greater than two by using a frequency multiplier in the feedback.
- Frequency multiplier can represent non-linearities present in the circuit.
- We can describe an Injection-locked Frequency Divider (ILFD) using a generalized mixer-based model similar to Miller's, since the locking mechanisms are identical.

Generalized Model for Injection-locked Divider



MIXER

- Single-balanced mixer based on a differential-pair
- Injected ω_{RF} into the tail device ("Injector"), which produces an RF current that adds to I_{BIAS}
- RF current may include a DC component and all harmonics of ω_{RF} For now, we will ignore this effect.

LOOP FILTER

- Mixer products are low-pass filtered and amplified by $H(j\omega)$
- Suppress mixer products > ω_0
- For small *n*, the output voltage V_O is sinusoidal.

Generalized Model for Injection-locked Divider (II)

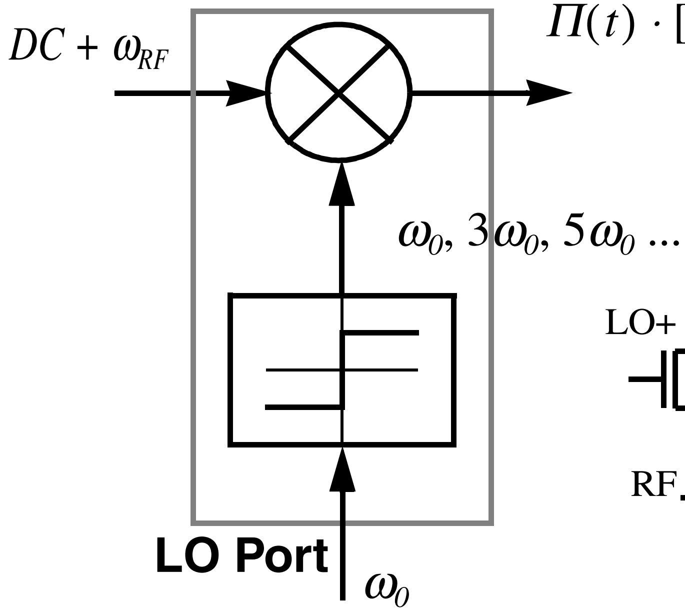
Use describing function analysis to determine the open-loop transfer characteristic's phase and magnitude components.

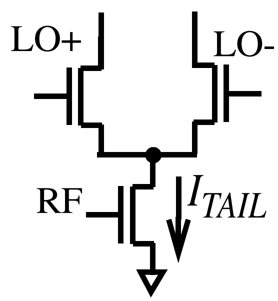
ASSUMPTIONS

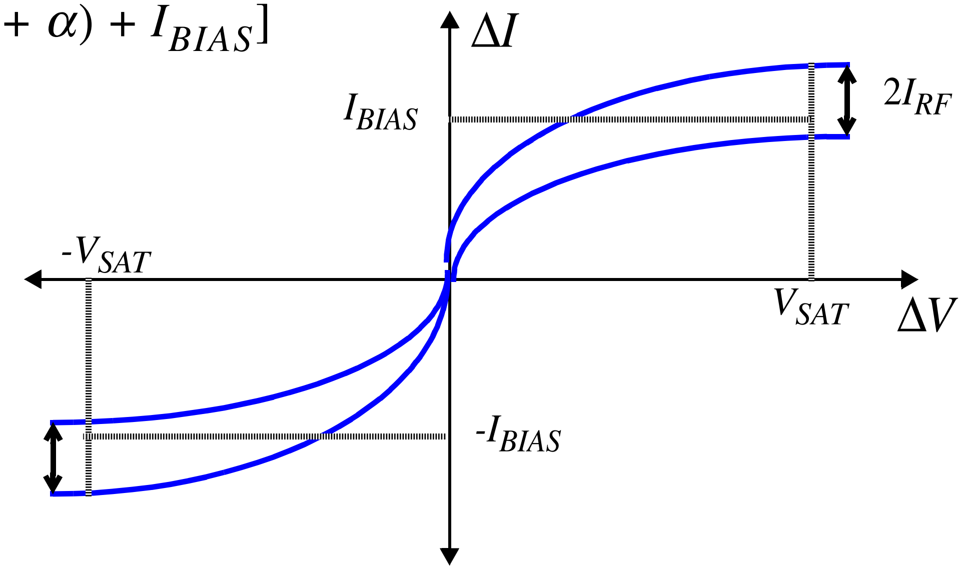
- If V_O is large, then the injection locking dynamics are determined by the phase relationship around the loop (phase-limited) and therefore we can ignore the amplitude expression.
- A large amplitude is also required to excite the Mixer's LO port non-linearity, which is the mechanism that makes possible division ratios greater than two.

Mixer

$$\Pi(t) \cdot [I_{RF} \cdot \cos(\omega t + \alpha) + I_{BIAS}]$$







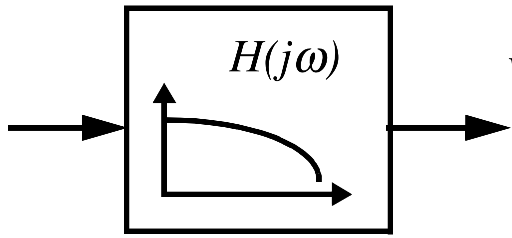
ASSUME $V_O \gg V_{SAT}$ (SWITCH HARD)

- The differential-pair's transfer characteristic is non-linear with odd symmetry.
- When excited by ω_0, the mixer's non-linearity produce odd harmonics at $3\omega_0$, $5\omega_0$, etc.
- The total current I_{TAIL} is modulated by ω_0 and its harmonics (square wave).

Fourier Coefficients of Mixing Function (Square Wave)

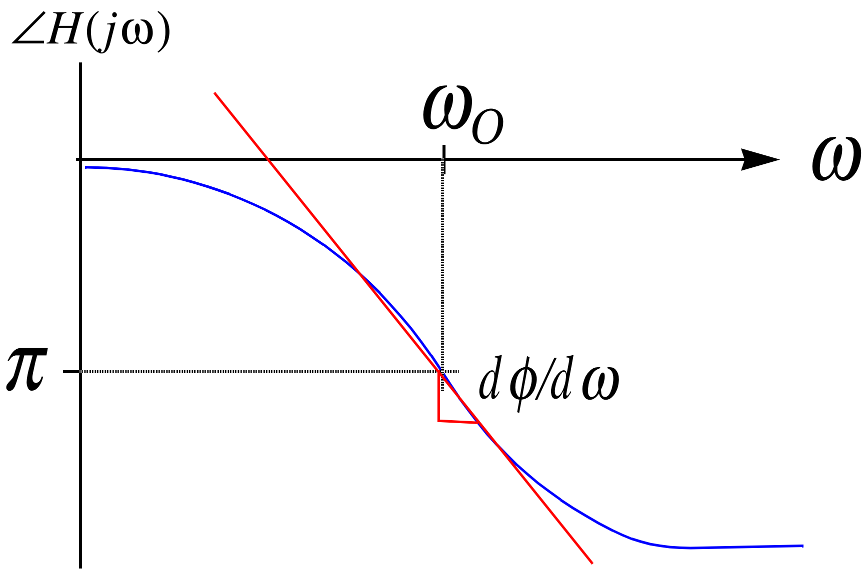
$$C_k = \begin{cases} \dfrac{1}{k\pi} \cdot (-1)^{(k-1)/2} & \text{for } k = odd \\ 0 & otherwise \end{cases}$$

Loop Filter



$$V_O \begin{cases} \omega_0 \\ |\omega_{RF} - (M+1)\omega_0| \\ |\omega_{RF} - (M-1)\omega_0| \end{cases}$$

$$H(j\omega) = \frac{H_O^n}{\left(1 + j\frac{\omega}{\omega_o}\tan\left(\frac{\pi}{n}\right)\right)^n}$$



LINEARIZE PHASE OF *H(jω)*

$$\angle H(j\omega) \cong \pi + \frac{n\sin\left(\frac{2\pi}{n}\right)}{2} \cdot \frac{\Delta\omega}{\omega_0}$$

$$\Delta\omega = \omega - \omega_O$$

- ω_0 is the frequency of the free-running oscillator.
- Each stage contributes π/n to the phase.

Locking Range of Injection-locked Ring Oscillator

WRITE PHASE EXPRESSION AROUND THE LOOP

$$\operatorname{atan}\left(\frac{\eta_i(C_{M-1}-C_{M+1})\sin\alpha}{C_1+\eta_i(C_{M-1}+C_{M+1})\cos\alpha}\right) = \angle H(j\omega)-\pi \qquad \eta_i = \frac{I_{RF}}{2I_{BIAS}}$$

MIXER **FILTER** **INJECTION EFFICIENCY**

LOCKING RANGE

$$\frac{\Delta\omega}{\omega_0} \cong \frac{4}{n\sin\left(\frac{2\pi}{n}\right)}\operatorname{atan}\left(\frac{k_0}{\sqrt{1-k_1^2}}\right)$$

$$k_0 = \eta_i\left|\frac{C_{M-1}-C_{M+1}}{C_1}\right|$$

$$k_1 = \eta_i\left|\frac{C_{M-1}+C_{M+1}}{C_1}\right|$$

Trade-offs

- The locking range is a function of injection efficiency η_i, and the magnitude of the Fourier coefficients C_{M-1} and C_{M+1}.
- For small values of injected signal the locking range increases linearly with the injected signal strength.

What Happens When Assumptions Break Down

1. **Limited Mixer Gain -** Switching function is not a square wave. (Swing ratio should be large, $\rho_s = V_0/V_{SAT} >> 1$)

- As ρ_s gets smaller, the square wave assumption is no longer valid and the coefficient ratios C_k/C_1 are significantly smaller.

2. **Limited Injection Efficiency -** Due to short-channel effects, velocity saturation, device non-linearity.

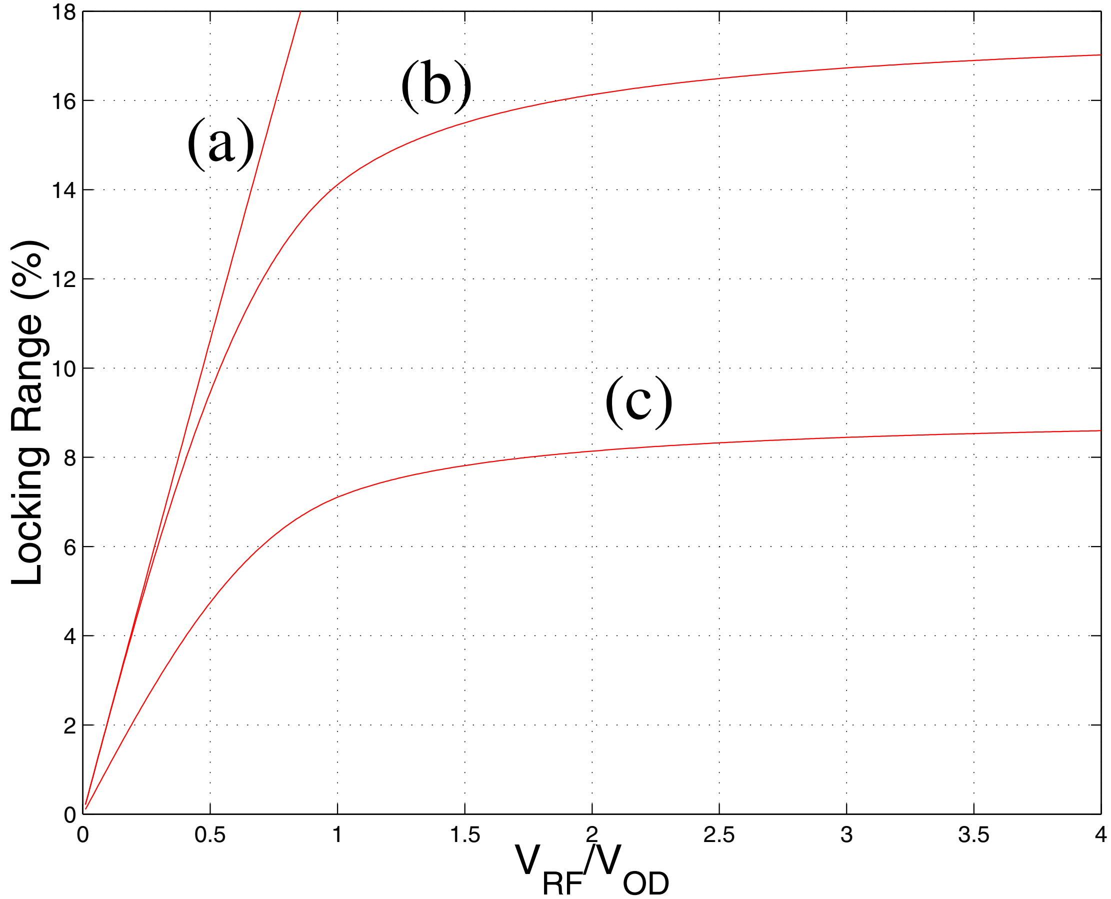
- Due to Injector non-linearities, I_{DC} rises for large injected signals ($I_{DC} > I_{BIAS}$). An increase of I_{DC} also affects V_{SAT}, reducing the swing ratio.

$$\eta_i = \frac{I_{RF}}{2I_{DC}} = \frac{V_{RF}}{2V_{OD,\,TAIL}} \cdot \gamma \qquad I_{DS} = K \cdot (V_{RF} + V_{OD,\,TAIL})^{\gamma}$$

3. **Mixer Tail Node Parasitics -** Due to tail drain junction and diffpair source junction.

- Parasitic capacitance at the drain of the tail device provides a shunt path for I_{RF} reducing η_i at high frequencies.

5-stage Ring Oscillator, modulo-8 Divider



(a)Ideal (phase-limited) case

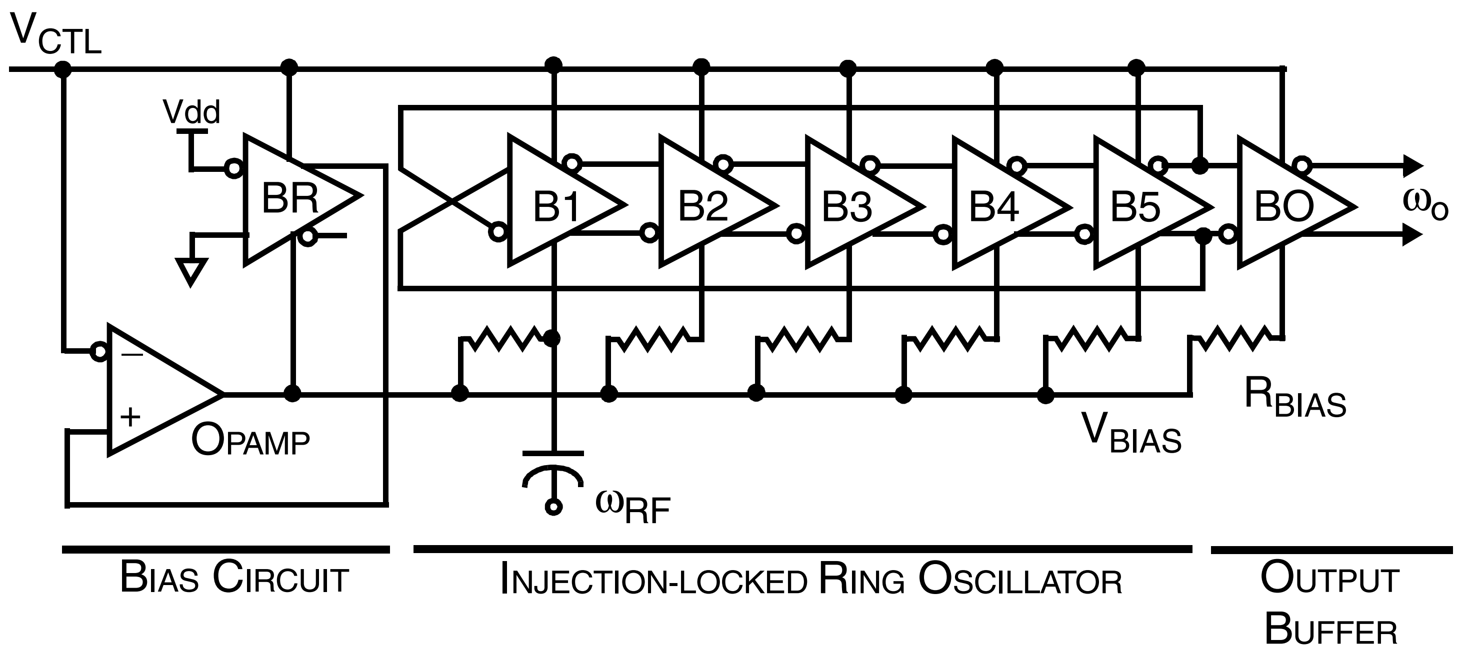
(b)Compression due to Injector non-linearity

(c)Effect of Injector non-linearity and drain junction parasitics (50% RF current loss)

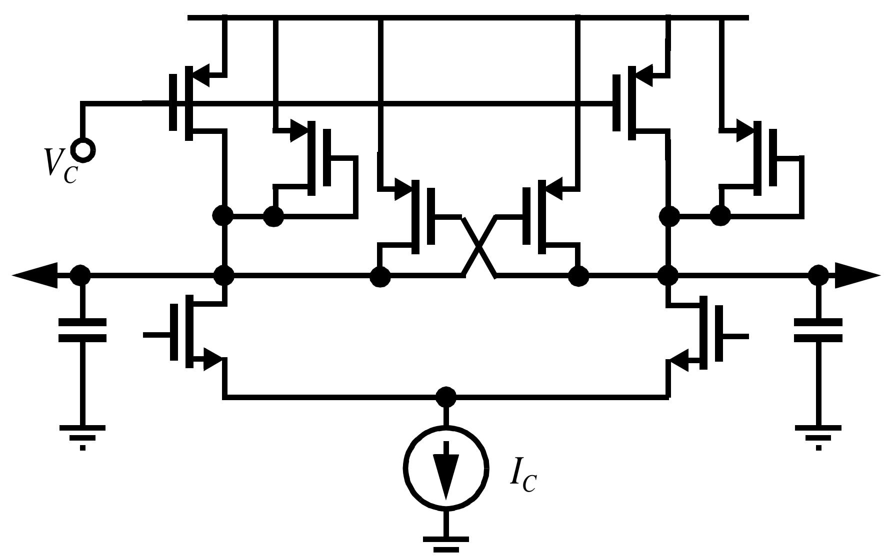
Outline

- Goals
- Ring Oscillator Overview
- Injection Locking Theory
- ***Circuit Implementation***
- Measured Results
- Conclusion

5-stage Injection-locked Ring Oscillator Divider



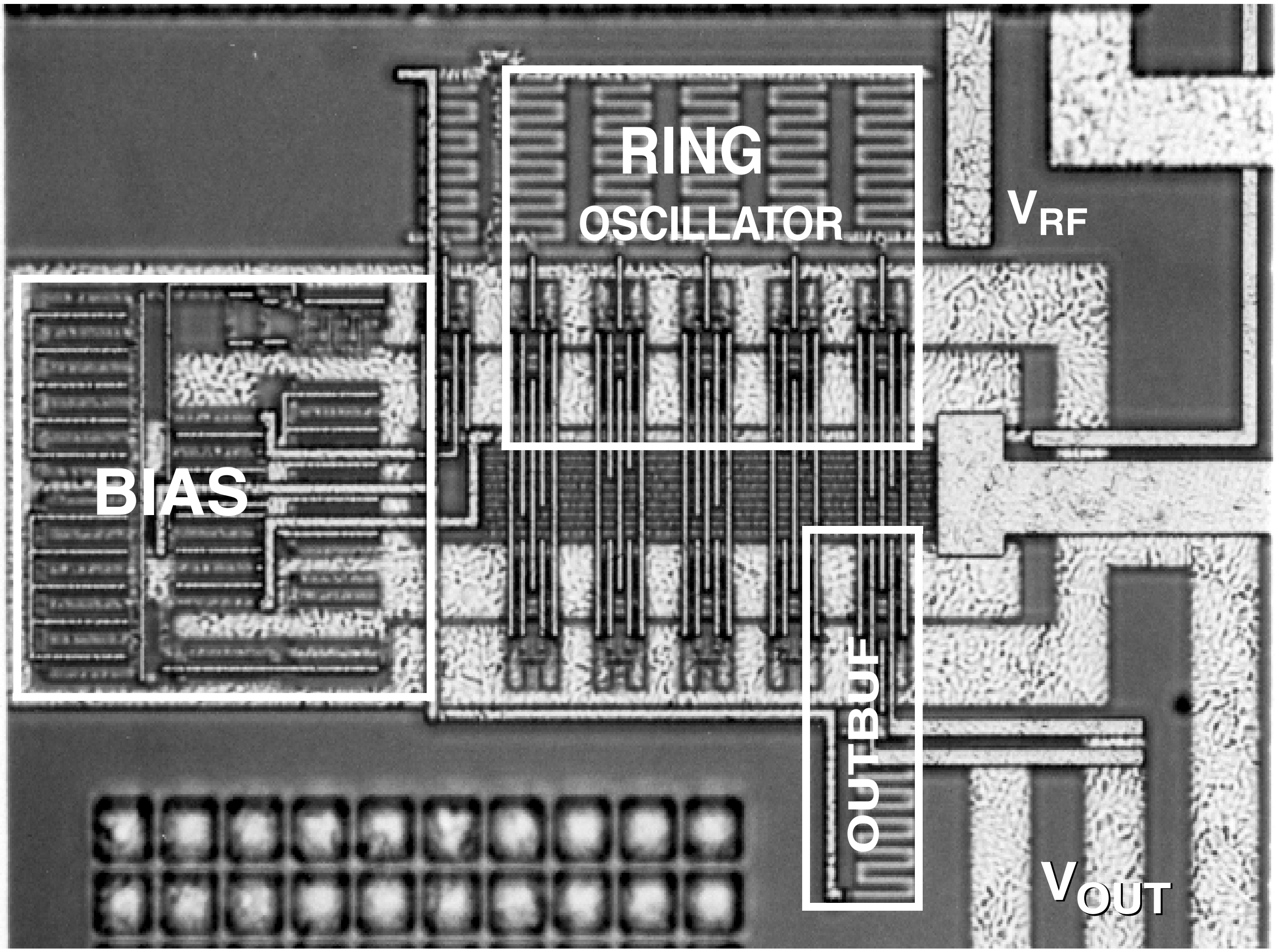
- Modified cross-coupled symmetric load buffers were used for their good supply noise rejection and low *1/f* noise upconversion characteristics.
- We injected the RF signal at the tail current source of the first buffer, using it as a single-balanced mixer.
- The buffer stages behave as the multipole filter $H(j\omega)$ that contribute the gain and phase shift required to sustain the oscillation.



Outline

- Goals
- Ring Oscillator Overview
- Injection Locking Theory
- Circuit Implementation
- ***Measured Results***
- Conclusion

Die Micrograph: 5-stage Ring Oscillator Divider



- Two ring oscillators were designed, with 3 and 5 buffer stages respectively.
- Layout is symmetrical and load balanced to avoid any skewing between the phases.
- 0.24-µm CMOS
- 0.012 mm^2 of area

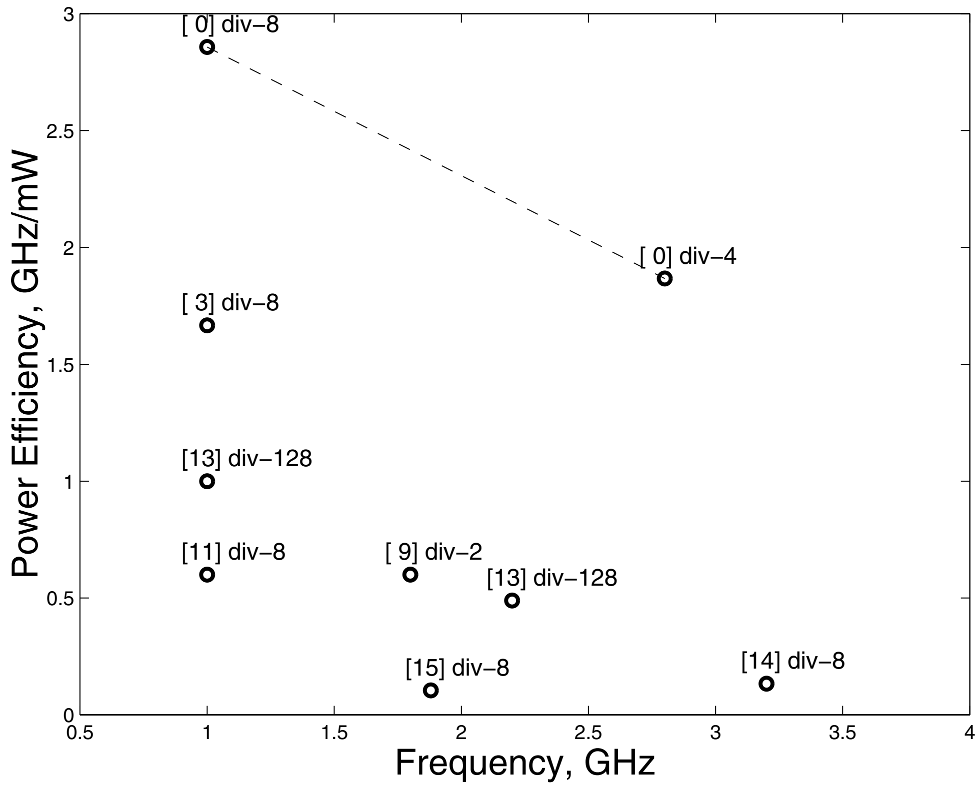
Results

Measurements

	5-stage ILFD	*3-stage ILFD*
Injected Frequency	1.0 GHz	2.8 GHz
Free-running Frequency	125 MHz	700 MHz
Phase Noise@100KHz	-110 dBc/Hz	-106 dBc/Hz
Locking Range		
Modulo-2	12.7 MHz (-3dBm)	125 MHz (-3dBm)
Modulo-4	32 MHz (-3dBm)	56 MHz (-5dBm)
Modulo-6	17 MHz (-3dBm)	no-lock
Modulo-8	20 MHz (-3dBm)	no-lock
Power dissipation		
Vdd	1.5 V	3.0 V
Icore	233 μA	331 μA
Ibias	108 μA	661 μA
Core power	350 μW	993 μW
Power efficiency	2.86 GHz/mW	2.82 GHz/mW

- Swing is smaller than expected, hence the locking range is smaller than predicted.
- Locking range is not symmetric around the free-running frequency of the ILFD, specially at higher injected power levels. This behavior is due to the increase of I_{DC} with the injected signal.

Power Efficiency of Injection-locked Ring Oscillator



- Power efficiency is the ratio of the divider's maximum operation frequency to its power dissipation expressed in GHz/mW.
- To achieve a fair comparison of the available data, only the "core" divider circuit is taken into consideration
- 5-stage (mod-8), 2.86 GHz/mW @1GHz.
- 3-stage, (mod-4), 2.82 GHz/mW @2.8GHz.

EXCEED ALL PUBLISHED RESULTS AT COMPARABLE FREQUENCIES

What We Learned

- Need to scale down the Injector to lower the parasitics, thus increasing the injection efficiency.
- The tail node parasitics can also be cancelled by resonating with an inductor (shunt-peaking), but this is not practical at sub-GHz frequencies.
- Increase the output swing and the *W*/*L* ratio of the Injector, hence increasing the swing ratio. This should be weighted against the resultant increase in parasitic capacitance and power dissipation.
- While a flip-flop based divider uses more power as we add more stages, the injection-locked divider uses less power for higher division ratios (every stage is operating at ω_0).

Outline

- Goals
- Ring Oscillator Overview
- Injection Locking Theory
- Circuit Implementation
- Measured Results
- ***Conclusion***

Conclusion

- Reviewed the operation of voltage-controlled CMOS ring oscillators.
- Described the injection locking mechanism and how it applies to CMOS ring oscillators.
- Showed the design of frequency dividers that can operate up to 2.8-GHz by exploiting the injection locking phenomena in differential CMOS ring oscillators.
- Showed measured results for 1-GHz and 2.8-GHz injection-locked frequency dividers fabricated in a 0.24-μm CMOS technology.
- Achieved the highest power efficiency (2.86 GHz/mW) ever reported in the literature.

References

1. A. Hajimiri and T.H. Lee, “A General Theory of Phase Noise in Electrical Oscillators,” *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, February 1998.
2. R.J. Betancourt-Zamora, T.H. Lee, “CMOS VCOs for Frequency Synthesis in Wireless Biotelemetry”, *Int’l Symp. Low Power Electronics & Design*, pp. 91-93, August 1998.
3. H. Darabi, A. Abidi, “A 4.5-mW 900-MHz CMOS receiver for wireless paging,” *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1085-96, August 2000.
4. H. Rategh, H. Samavati and T.H. Lee, “A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5GHz Wireless LAN Receiver,” *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 780-787, May 2000.
5. J. Maligeorgos, J. Long, “A 2-V 5.1-5.8 GHz Image-reject Receiver with Wide Dynamic Range,” *Int’l Solid-State Circuits Conf.*, pp. 322-323, 468, February 2000.
6. S. Kudszus, W.H. Haydl, et. al, “94/47-GHz Regenerative Frequency Divider MMIC with Low Conversion Loss,” *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1312-17, September 2000.
7. K. Washio, E. Ohue, et. al, “82-GHz Dynamic Frequency Divider in 5.5-ps ECL SiGe HBTs,” *Int’l Solid-State Circuits Conf.*, pp. 210-211, 458, February 2000.
8. R.L. Miller, “Fractional-Frequency Generators Utilizing Regenerative Modulation,” *Proc. IRE*, vol. 27, pp. 446-457, July 1939.

References (II)

9. H.R. Rategh and T.H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813-821, June 1999.

10. J.G. Maneatis, "Low-Jitter and Process-independent DLL and PLL based on Self-biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, November 1996.

11. C.S. Vaucher, I. Ferencic, et. al, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-um CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039-45, July 2000.

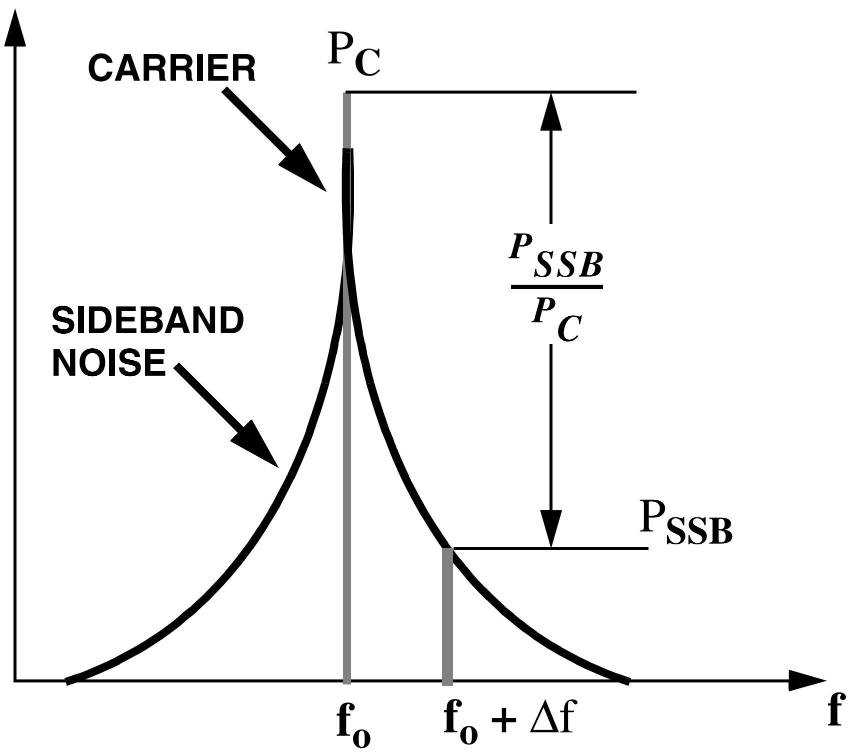
12. H. Wu, A. Hajimiri, "A 19-GHz, 0.5-mW, 0.35-um CMOS Frequency Divider with Shunt-Peaking Locking-Range Enhancement," *Int'l Solid-State Circuits Conf.*, February 2001.

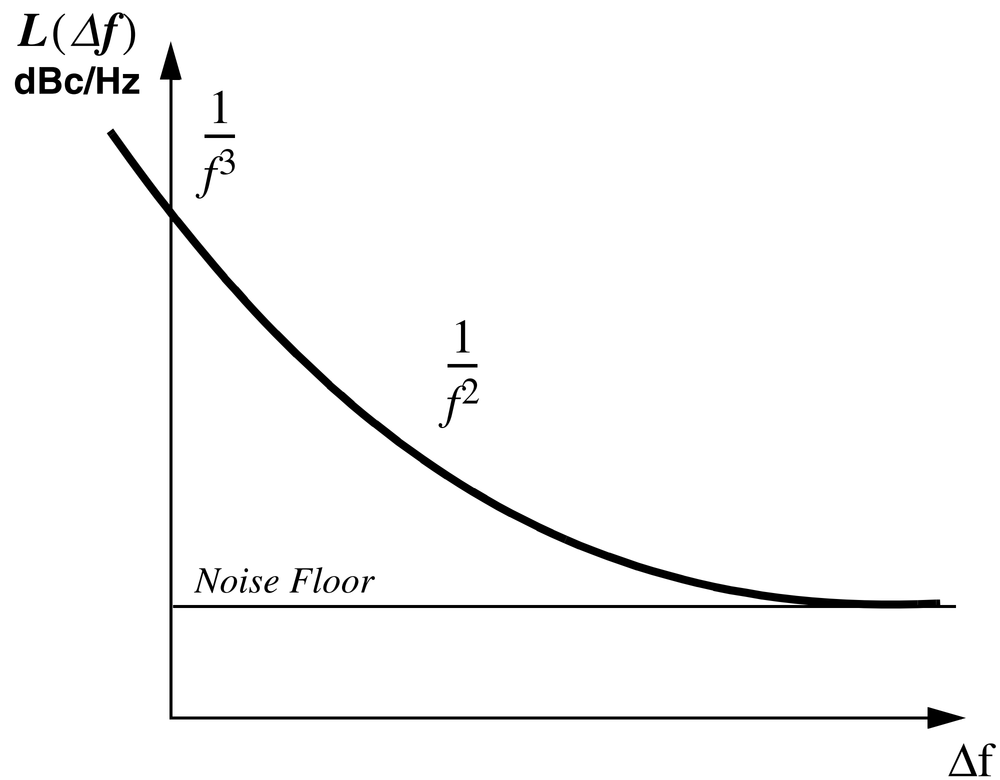
13. Y. Kado, T. Ohno, et. al, "An Ultralow Power CMOS/SIMOX Programmable Counter LSI," *IEEE J. Solid-State Circuits*, vol. 32, no. 10, pp. 1582-87, October 1997.

14. Y. Kado, Y. Okazaki, et. al, "3.2 GHz, 0.2 um Gate CMOS 1/8 Dynamic Frequency Divider," *Electronic Letters*, vol. 26, no. 20, pp. 1684-86, September 1990.

15. J. Craninckx, M. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7-um CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 890-897, July 1996.

What is Phase Noise?



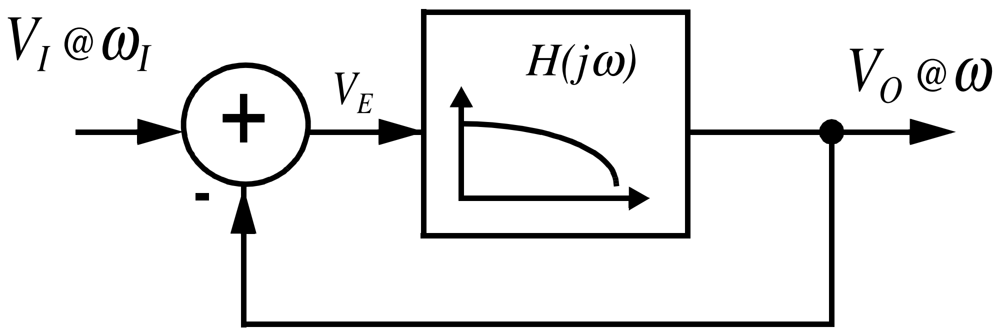


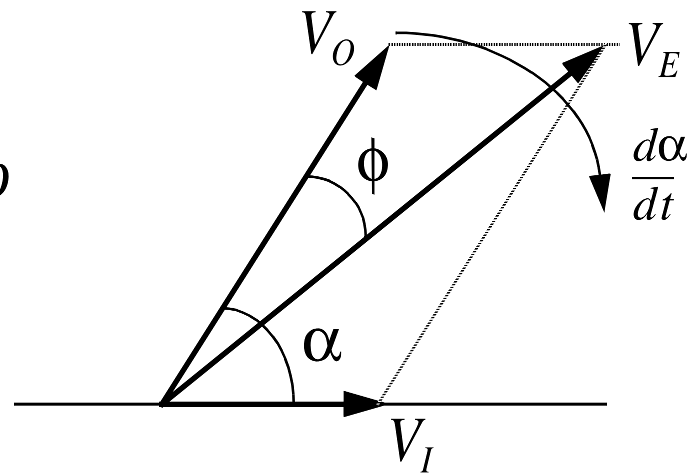
- Undesirable phase fluctuations due to intrinsic device noise
- Output power is not concentrated at the carrier frequency alone

- Phase noise is represented as a ratio of power in 1Hz bandwidth in one sideband to the power of the carrier.
- Specified in dBc/Hz at a frequency offset from the carrier.

What is Injection Locking? [Adler 1946]

ASSUME $\omega_I \approx \omega_O$ **AND** $V_I << V_O$



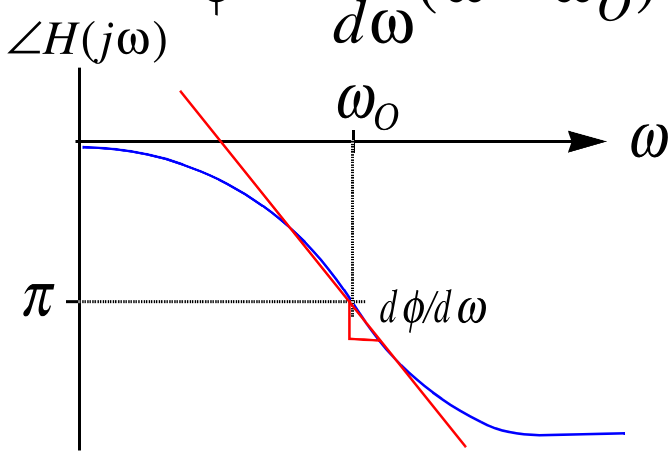


$$\phi = \angle H(j\omega) + \pi$$

LINEARIZE PHASE

$$\phi = \frac{d\phi}{d\omega}(\omega - \omega_O)$$

$$\omega = \omega_I + \frac{d\alpha}{dt} \qquad \phi = -\frac{V_I}{V_O}\sin\alpha$$



$$\omega = \frac{-V_I/V_O \sin\alpha}{d\phi/d\omega} + \omega_O$$

- Output frequency shifts from free-running frequency
- **IF** $V_I = 0$ **THEN** $\phi = 0$ and $\omega = \omega_O$

Locking Range of Injection-locked Oscillator

1. FREQUENCY SHIFT

$$\omega = \frac{-V_I/V_O \sin\alpha}{d\phi/d\omega} + \omega_O$$

$$\omega = \omega_I + \frac{d\alpha}{dt}$$

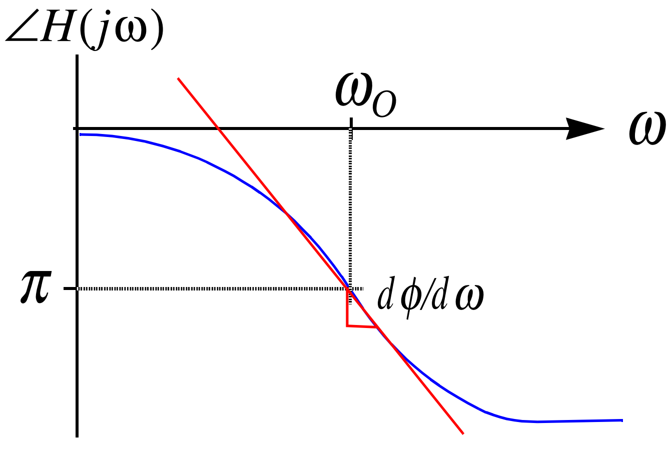
2. DIFFERENTIAL EQUATION

$$\frac{d\alpha}{dt} = \frac{-V_I/V_O \sin\alpha}{d\phi/d\omega} + \Delta\omega_O$$

$$\Delta\omega_O = \omega_O - \omega_I$$

3. LINEARIZE PHASE OF *H(jω)*

$$\frac{d\phi}{d\omega} \cong \frac{n}{2\omega_O}\sin\left(\frac{2\pi}{n}\right)$$



4. STEADY-STATE SOLUTION

FOR $\frac{d\alpha}{dt} = 0$

LOCKING RANGE

$$\left|\frac{\Delta\omega_O}{\omega_O}\right| < \frac{V_I}{V_O} \cdot \frac{2}{n\sin\left(\frac{2\pi}{n}\right)}$$

