INJECTION-LOCKED RING OSCILLATOR FREQUENCY DIVIDERS

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Abstract

In this thesis, we propose a technique that has the potential of reducing the power dissipation of frequency division by up to an order of magnitude compared to conventional digital solutions by exploiting injection-locking in CMOS ring oscillators. Injection locking—the synchronization in frequency and phase of a free running oscillator with a source—is a mechanism that has been observed and studied since the early days of radio. In this work we use injection-locking in differential CMOS ring oscillators to implement frequency prescalers that can operate at frequencies up to 2.8 GHz. We also present a low-power technique, the injection-locked loop, that extends the natural locking range of ring oscillator frequency dividers.

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Chapter 1

Introduction

Some are called smart tags, others radios-on-a-chip (ROCs), some other go by code names such as IEEE-802.11 or Bluetooth. They are meant to connect all computers, handheld devices and peripherals. They give us the freedom to roam about the building with our laptops, PDAs, pagers, etc. But, what are these devices and why should we care about them?

Recently there has been extreme interest in short-haul low-power radio systems. A low-power, radio-on-a-chip (RoC) that requires no external components can enable novel applications that are not economically feasible otherwise. With current complementary metal-oxide-semiconductor (CMOS) silicon technology we can fit all the major components of a radio transmitter and receiver in a square millimeter of area. A CMOS chip radio of this size would cost about 10 cents to manufacture. The small cost of this device opens up possibilities for uses in applications not possible before due to economic factors.

For instance, a pacemaker could communicate with a PDA and send an alarm to the hospital over the Internet (Figure 1-1). We could also monitor the

Figure 1-1 Applications of a radio-on-a-chip (RoC)

health condition of a baby in-utero. A smart sensor could be embedded into a building constantly monitoring the stress in the structure. Disposable merchandise tags could be interrogated wirelessly in a store allowing instant inventory counts. Applications are endless.

Our research goal is to develop techniques that will allow the design and construction of a very small radio receiver that will be suitable for these applications. Applications that will benefit the most from this technology require a range of up to 10 meters while using either the 900-MHz or the 2.4-GHz unlicensed ISM (industrial, scientific, and medical) frequency bands. Depending on the application we may also need the radio to operate for hundreds of hours using only a small battery. The key parameter of these system is power dissipation. Power dissipation and battery lifetime determine the size of the battery which ultimately determines the size of the device.

A significant portion of the power budget for any RoC system is allocated to the generation of the RF carrier and local oscillator (LO). The LO generates a high frequency signal used to downconvert the signal we are interested in receiving. Figure 1-2 shows a typical CMOS radio receiver operating in the

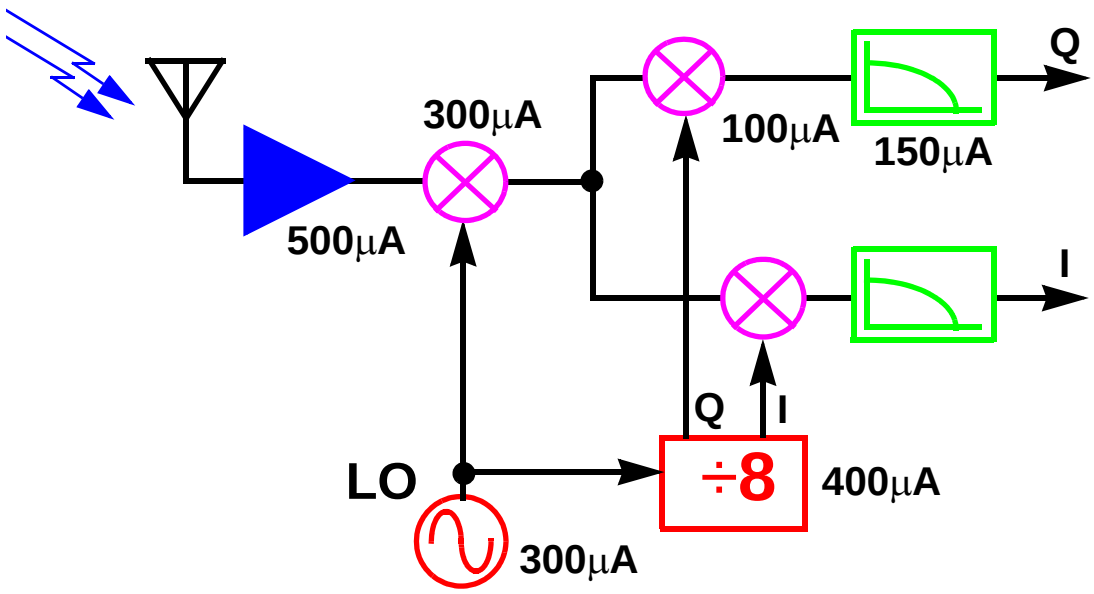

Figure 1-2 900MHz CMOS Radio Receiver

900-MHz band [Darabi00]. To receive different channels, we need to control very precisely the frequency of the LO. We can observe that generating the different frequencies required for the downconversion mixers in this example consume a significant portion of the power budget.

Given this need for precise, low-power LO generation, a completely integrated frequency synthesizer is required. However, a frequency synthesizer is usually implemented using a phase-locked loop (PLL). A PLL is typically composed of a voltage-controlled oscillator (VCO), frequency divider (FD), and a phase detector in a feedback loop (Figure 1-3). The VCO generates the LO signal (FOUT), and its frequency is divided down by the FD so that it can be compared by the phase detector to a very precise, low-noise reference frequency (FREF) derived from a quartz crystal. In essence, the VCO frequency tracks the frequency of the quartz crystal, but at a multiple of the frequency divider ratio. The PLL also tracks the phase noise of the reference signal within its loop bandwidth, relaxing the close-in phase noise requirements of the VCO.

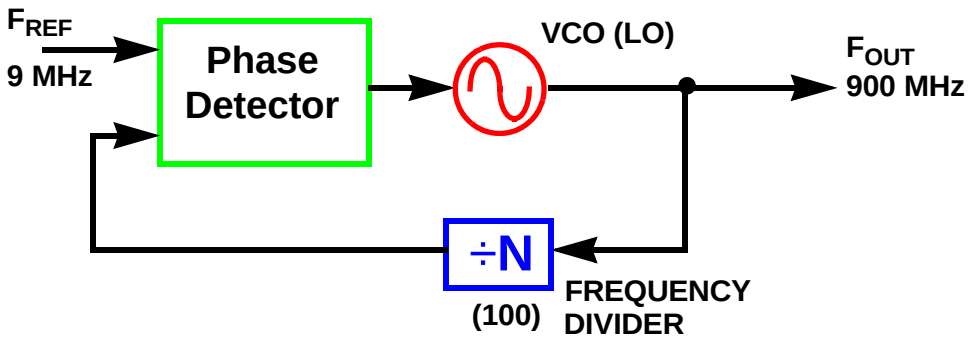

Figure 1-3 PLL Frequency Synthesizer Block Diagram

Another example of an integrated CMOS frequency synthesizer operating around 300MHz (Figure 1-4) illustrates the power allocation among the different components of a PLL [vKaenel96]. We can observe that the major sources of power dissipation in a frequency synthesizer are the VCO (800μA) and frequency dividers (290μA) which represent 73% and 22% of the total power budget respectively. The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required. Great efforts have been made recently in understanding the fundamentals of low-power operation for communications-grade integrated VCOs. There is still a great need for a better understanding of low-power techniques for frequency division which is essential to reduce the overall power dissipation. To this end, we have

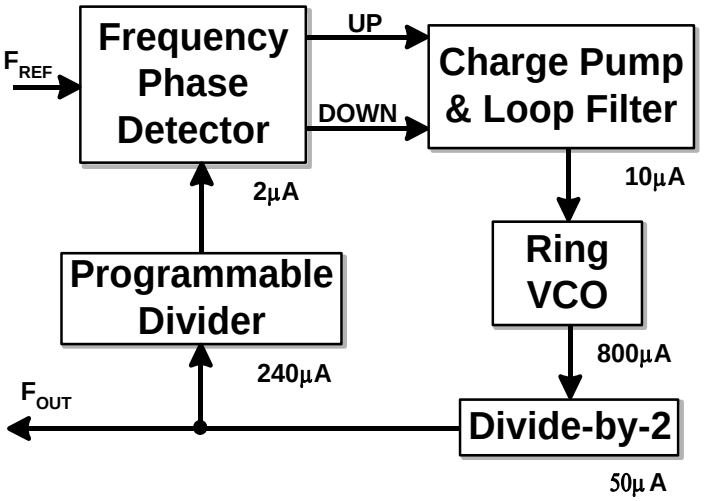

Figure 1-4 CMOS PLL Frequency Synthesizer for Clock Generation

developed techniques used to minimize the power dissipation of the PLL with a special emphasis in the VCO and frequency dividers.

1.1 Voltage-controlled Ring Oscillators

As we previously stated, oscillators are key building blocks in integrated radio transceivers. The main design challenge is to find the right topology that meets the frequency range, noise, area, power, and other requirements imposed by the transceiver. Ring oscillators are the simplest type of oscillator used in RFIC design. For instance, a ring oscillator can be constructed by employing a chain of three or more inverting amplifier stages where the output is fed back to the input. Oscillation will result and will be sustained for any number of odd stages.

In this investigation, we propose a methodology that uses a new phase noise model to trade-off phase noise and power dissipation in the design of ring oscillators suitable for RFIC frequency synthesis. We compare the phase noise performance of ring oscillators based on three distinct topologies, including a cross-coupled topology that achieves lower phase noise by exploiting symmetry. Chapter 3 describes in further detail the research, analysis and new design insights for low-power integrated high-frequency ring oscillators suitable for RFIC transceivers.

1.2 Injection-locked Frequency Dividers

Modern integrated CMOS frequency dividers are usually implemented using digital techniques such as fully static or dynamic flip-flops and current-mode logic (CML). These have the advantage of being insensitive to process variations, allowing for programmable division ratios, and having a small area,

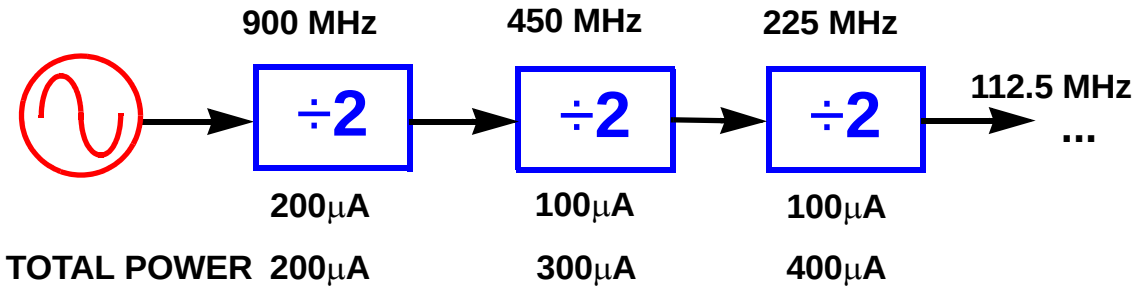

Figure 1-5 Digital CMOS Frequency Divider Trade-offs

making them easy to integrate. The major disadvantage is that the power dissipation increases with the division ratio (Figure 1-5) [Darabi00]. This drawback is most severe in the first few stages of a feedback divider in a PLL, where the frequency of operation is the highest.

We propose a technique that has the potential of reducing the power dissipation of frequency division by up to an order of magnitude compared to conventional digital solutions by exploiting injection-locking in differential CMOS ring oscillators. Injection locking is the synchronization in frequency and phase of a free running oscillator with a source. The mechanism of injection locking has been observed in a wide variety of oscillators and has been known for decades [vanderPol34]. In 1939 Miller proposed a regenerative frequency divider based on this principle [Miller39]. Miller's divider can achieve division ratios greater than two by using a frequency multiplier in the feedback loop. Injection-locked dividers have the counter-intuitive property that for a given input frequency, power dissipation decreases with increasing division ratio.

In this work we exploit injection-locking in CMOS ring oscillators to implement frequency dividers that can operate at frequencies of up to 2.8 GHz [Betancourt01]. These results are presented in more detail in Chapter 4.

1.3 Injection-locked Loop

Our experience with typical ring oscillator frequency dividers reveals that high-modulus operation comes at the expense of operating range. In order for the application of higher order moduli to be useful and practical, we need to extend the locking range of the divider.

As will be discussed in Chapter 2, even though we know that we can use the phase difference between input and output of an injection-locked system for frequency tracking, it is not always practical to do so if the output is at a different frequency from the input. For instance, the frequency multiplier of Kudsuz [Kudszus00a] uses a mixer to downconvert the output before comparing its phase with that of the injection signal. The inverse case of a frequency divider requires generating a harmonic of the output to compare with the injected signal. Direct phase detection thus requires a second path of frequency conversion, which makes it very cumbersome and inefficient. In theory we could also use a sampling phase detector, but again, it would require further processing at the higher input injection frequency. That extra overhead would negate the power savings of the ILFD at high moduli.

An important goal, then, is to perform phase comparisons without incurring too much overhead in terms of power and complexity. A relevant observation is that injection locked dividers implemented using quadrature ring oscillators (e.g., 4-stage differential) exhibit a deterministic deviation from quadrature due to the injected signal. That is, the extra phase that synchronizes the oscillator to the injected signal is detectable as an error in quadrature. This error is proportional to the deviation of the injected signal from the free running frequency of the oscillator. This is a key observation, as the ILL operates with signals at the *lower* output frequency, with a corresponding minimal impact on

power dissipation.

For PLL applications, enhancing the locking range with an ILL is not enough, as the ILFD needs to be locked in order for the ILL to track. The ILL works fine in extending the locking range, but it needs a frequency acquisition assist to initialize the loop. Making the free-running frequency of the PLL's "master" VCO track that of the "slave" ILFD is not trivial. Using ring oscillators is even more challenging, as the same control voltage needs to produce a different frequency in each of the oscillators. Typically, ring oscillator gain is ill-controlled over PVT corners, with a factor of two of variation not uncommon. Also, for frequencies that are two octaves apart, the slope of the curve changes significantly. So just matching the two VCOs is not enough. We can turn this problem around and lock the master to the slave instead. This tuning technique will be described further in Chapter 5.

1.4 Organization

This thesis is a compilation of several experimental investigations. Each major investigation is designed to refine techniques for lowering the power dissipation of frequency dividers based on injection-locked ring oscillators. Each major experiment is a separate chapter, with the exception of Chapter 2, which serves as a background chapter.

Chapter 2 presents a simple ring oscillator theory, along with an introduction to modeling of injection-locked processes. The historical development and applications of injection-locking to ring oscillators is also discussed.

Low-power ring oscillator design is presented in Chapter 3. Basic phase noise theory is also introduced. Here we discuss the design of low-power

differential CMOS ring oscillators suitable for RF frequency synthesis. We present experiments used to evaluate different ring oscillator topologies within the noise–power design envelope.

In Chapter 4, we study the injection-locking mechanism and how it can be exploited to achieve low-power frequency division using CMOS ring oscillators. We present experimental results that validate our models.

In Chapter 5, we introduce the concept of the injection-locked loop. We describe the evolution that led to its discovery and modeling.

In Chapter 6 we present our conclusions as well as recommendations for further work.

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Chapter 2

Background

This chapter presents a brief ring oscillator theory along with an introduction to modeling of injection-locked processes. The historical development and applications of injection-locking to ring oscillators is also discussed.

Two basic idioms familiar to CMOS RFIC designers are the ring oscillator and the LC oscillator. LC oscillators use resonators, whose energy losses are compensated by active elements such as MOS or bipolar transistors. The active elements also generate noise, usually in proportion to the amount of energy supplied to sustain oscillation. Provided that the quality factor[1] of the resonator is high, low noise LC oscillators can be made. However, designers of fully integrated CMOS LC oscillator usually have to struggle with the low quality factor and large area of the monolithic spiral inductors typically available in standard CMOS processes. Moreover, large, lossy, on-chip resonators at sub-GHz frequencies negate many of the benefits of using LC oscillator topologies.

Third, oscillators not based on resonator topologies, such as ring

1. The *quality factor* (Q) of a resonator is proportional to the ratio of energy stored to the energy dissipated, per unit time.

oscillators[2], generally have poor spectral purity compared to LC oscillators of similar power budgets. However, with its large tuning range, ease of integration, and relatively small silicon area, the ring oscillator is an attractive alternative for sub-GHz applications. This thesis focuses exclusively on the ring oscillator.

2.1 Ring Oscillator Primer

The main oscillator design challenge is to find a topology that meets the frequency range, noise, area, power, and other requirements imposed by the transceiver. This section describes the basic theory of operation of high-frequency ring oscillators suitable for CMOS RFIC transceivers.

Ring oscillators are the simplest type of oscillator used in RFIC design - a ring oscillator can be constructed using a chain of three or more single-ended inverters where the output of the last stage is fed back to the input of the chain (Figure 2-1). Moreover, ring oscillators are usually incorporated on-chip for quality monitoring of the semiconductor manufacturing process. For example, a 31-stage minimum size inverter-based ring oscillator is used by the MOSIS service as part of their CMOS process monitor [MOSIS04]. The ring oscillator frequency is a simple performance benchmark useful for comparing various foundry technologies. Moreover, it serves as a crude check on extracted simulation model parameters.

Intuitively, the oscillation period corresponds to the time it takes a transition to propagate twice around the loop. A power-on transient or thermal

2. Low-swing (or current limited) ring oscillators can be classified as non-resonant phase shift oscillators. In the large signal regime (voltage limited), a relaxation model better describes their behavior.

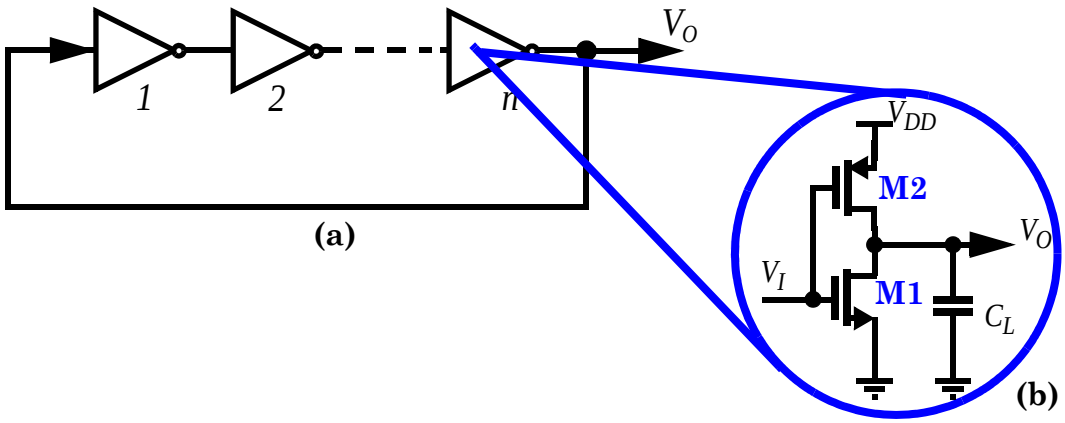

Figure 2-1 CMOS ring oscillator model: (a) block diagram for n-stage single-ended ring oscillator; (b) circuit diagram for a static CMOS inverter

noise suffice to start oscillations, even if all the stages happen to power up in the balanced state right at their switching threshold[3].

In the context of digital design, the oscillation frequency of the ring oscillator may be approximated by

$$f_{OSC} \cong \frac{1}{2nT_D}, \tag{2-1}$$

where n is the number of stages and T_D is the propagation delay[4] through each inverter. Oscillation may be sustained for any number of odd stages, as will be shown shortly. Furthermore, the propagation delay T_D is sensitive to variations in process, supply voltage, and temperature (PVT) and is thus best characterized with transistor-level simulation using accurately extracted device models.

2.1.1 Linear Time-Invariant Model

In the rest of this section, we present a simplified linear time-invariant

3. In practice, this condition never happens (even in perfectly balanced ring oscillators) as random mismatches will make the switching threshold of each stage slightly different from the others.
4. Propagation delay is the time required for the output of a gate to respond to a combination of its inputs. It is measured between the points where the input and output cross 50% of their final value.

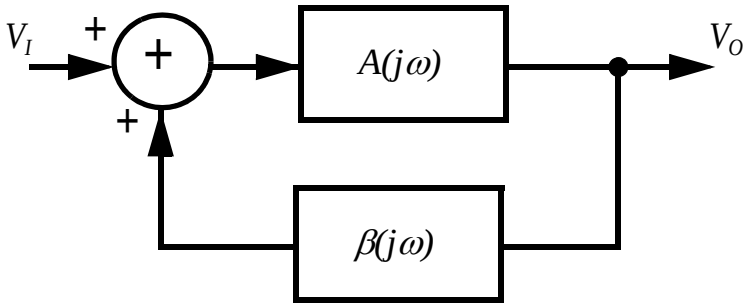

Figure 2-2 Canonical feedback system

(LTI) model to gain insight into the operation of the ring oscillator. In this approach, the nonlinear relationships are approximated by a first-order Taylor expansion around a fixed bias point, resulting in an LTI small-signal model. An LTI model enables the use of Laplace transforms and a description of the system dynamics in terms of the poles and zeros of the transfer function. If the amplitude of the signals is small compared to the bias point, the description is accurate. Therefore, this model will be useful for predicting the oscillation start-up conditions as well as the behavior while the signals are relatively small. Even though there will be significant error in trying to predict large signal behavior using this approach, we nevertheless gain significant design insight from this exercise.

The canonical form of a feedback system is shown in Figure 2-2, where the upper branch $A(j\omega)$ represent active elements, $\beta(j\omega)$ models a passive feedback network. The following equation describes its transfer function

$$\frac{V_O(j\omega)}{V_I(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)\cdot\beta(j\omega)}, \qquad (2\text{-}2)$$

where the product $A(j\omega)\beta(j\omega)$ is the open loop gain. The feedback will be referred to as either *positive feedback* or *negative feedback* according to the absolute value of $1/(1-A(j\omega)\beta(j\omega))$ being either greater or less than unity [Black34].

The system can become unstable when $1 - A(j\omega)\beta(j\omega) = 0$. When this condition is satisfied, the closed loop gain becomes infinite. Furthermore, noise (present in any physically realizable amplifier) may cause an exponential increase in oscillation amplitude at the frequency where this condition is met. In practical amplifiers there is gain compression in the active devices as the output voltage approaches either power rail. The drop in loop gain thus limits the amplitude of oscillation. The necessary conditions for oscillation just described are known as the Barkhausen criteria[5] and can be expressed in terms of magnitude and phase of the open loop transfer function by

$$|A(j\omega) \cdot \beta(j\omega)| \geq 1 \tag{2-3}$$

$$\angle A(j\omega) \cdot \beta(j\omega) = 180°. \tag{2-4}$$

In practice, ring oscillators are constructed using a chain of digital inverters with an odd number of inversions, where the output of the last stage is connected to the input of the first one, as shown in Figure 2-1(a). For illustration purposes, we assume that each amplifier stage uses the simple NMOS inverter shown in Figure 2-3(b) with a transfer function given by Equations (2-2) through (2-6):

$$A(j\omega) = A_o \frac{(1 - s/\omega_z)}{(1 + s/\omega_p)} \cong A_o \frac{1}{(1 + s/\omega_p)} \tag{2-5}$$

$$A_o = -g_m \cdot R_L \tag{2-6}$$

$$\omega_p = \frac{1}{R_L \cdot C_L} \tag{2-7}$$

$$\omega_z = \frac{g_m}{C_{GD}} \tag{2-8}$$

$$C_L = C_{GS} + (2 + g_m \cdot R_L) \cdot C_{GD} + C_{DB}. \tag{2-9}$$

5. In 1911, German physicist Heinrich Georg Barkhausen (1881-1956) was appointed to the world's first professorship in communications (electrical engineering) at the Technical Academy in Dresden, where he worked on theories of spontaneous oscillation and nonlinear switching elements. In 1920, he co-developed the *Barkhausen-Kurz* UHF oscillator, an early microwave tube. (source: Encyclopædia Britannica Online.)

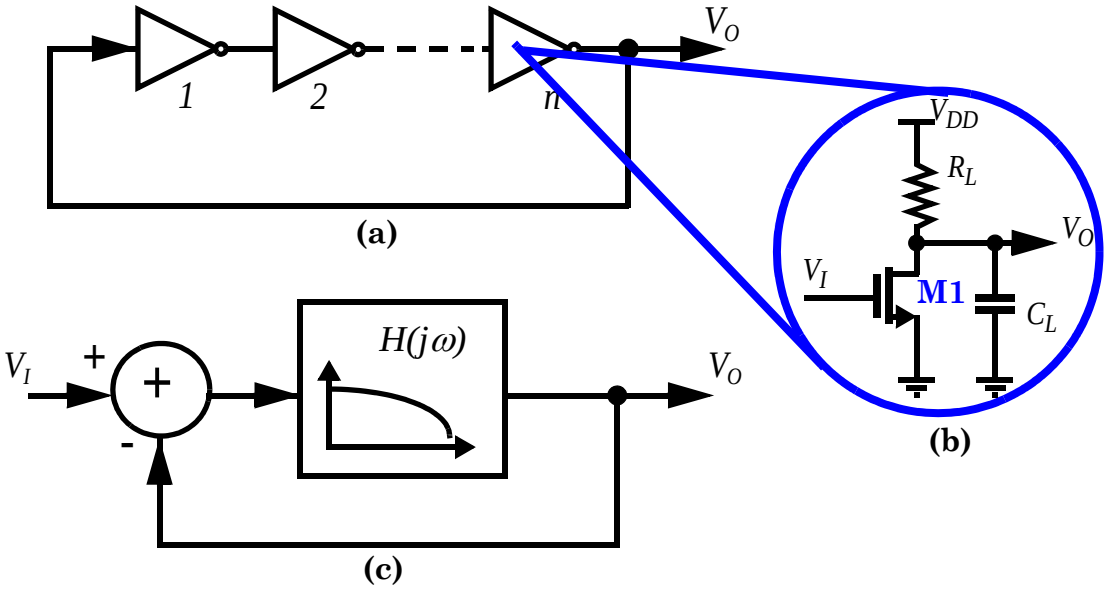

Figure 2-3 Ring oscillator model: (a) block diagram for n-stage single-ended ring oscillator; (b) simplified circuit diagram for an NMOS inverter; (c) LTI ring oscillator model

The DC gain of the inverter is given by product of the transconductance g_m of the NMOS device M1 and the output load resistance (neglecting the output resistance of M1). We observe that there is an output pole (ω_p) due to the interaction of the ouput load resistance R_L with the load capacitance C_L. The load capacitance C_L is composed of the input gate capacitance C_{GS} and Miller-multiplied gate-drain overlap capacitance of the next stage, as well as the parasitic drain difussion capacitance C_{DB}. Furthermore, there is a right-half plane (RHP) zero (ω_z) that introduces a phase lag into the transfer function due to the feedforward signal path caused by C_{GD}. In most cases, the RHP zero will be at a high enough frequency that its effect can be neglected. Moreover, this model is also valid for differential NMOS amplifiers, where g_m is the transconductance of the differential pair.

Figure 2-3(c) shows the corresponding LTI model where the open loop transfer function $H(j\omega)$ models the low-pass filtering action of n amplifier

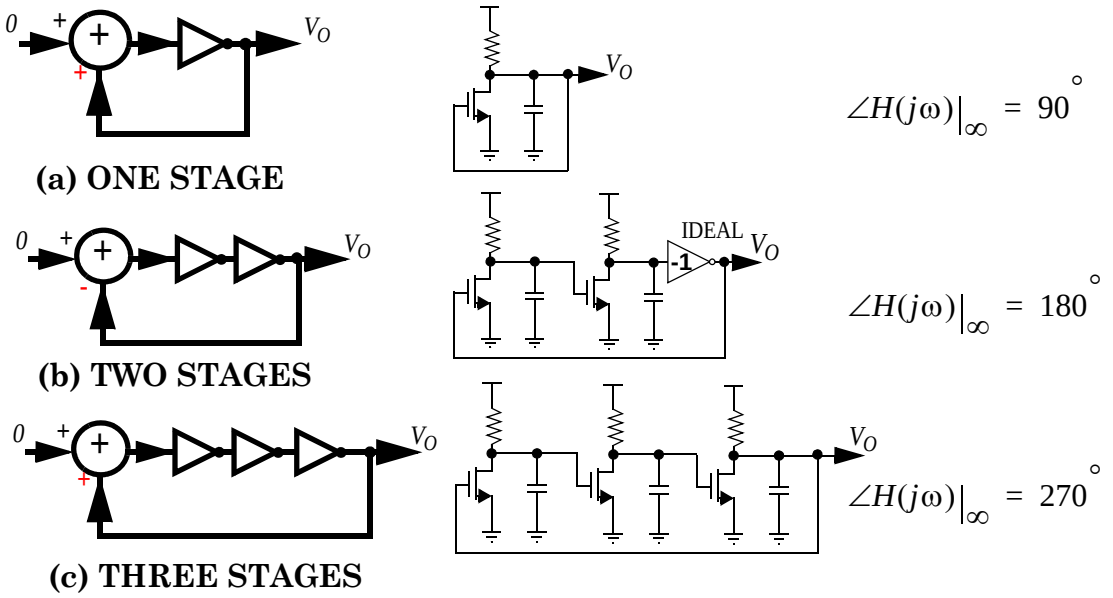

Figure 2-4 Evolution of the ring oscillator: (a) One stage; (b) Two stages; (c) Three stages.

stages due to the interaction of the output impedance of each buffer with the input capacitance of the following stage. The output at V_0 is fed back to the input port, thus closing the feedback loop. Note that for odd values of n, there is one net inversion around the loop.

To quantify the startup conditions of the ring oscillator, first we determine the open-loop transfer characteristic and separate it into phase and magnitude components. For oscillation, the open loop transfer function for an n-stage chain of inverters must meet the Barkausen criteria as shown in equations (2-7) and (2-8).

$$H_o \geq \sqrt{1 + \tan\left(\frac{\pi}{n}\right)^2} \tag{2-10}$$

$$\omega_p = \frac{\omega_0}{\tan\left(\frac{\pi}{n}\right)}, \tag{2-11}$$

where ω_o is the free-running frequency of the oscillator. Each stage contributes π/n to the phase, resulting in a total phase lag of 2π around the loop (including

the inversion). These equations are only valid for 2 or more stages.

Figure 2-4 illustrates qualitatively the ramifications of equations (2-7) and (2-8) for ring oscillators of increasing number of stages [Razavi00]. First, Figure 2-4(a) depicts a single inverter in a feedback loop. A single pole can contribute at most 90 degrees of phase shift (at infinite frequency), thus the system is always stable and no oscillation is possible. Second, Figure 2-4(b) shows a ring oscillator with two stages. In this case there is sufficient phase shift to cause oscillation, but only at infinite frequency. This condition also requires infinite loop gain. The simplifications in this analysis neglect the contribution of the feedforward zero and other higher order poles in the system. Given these additional effects, a practical 2-stage ring oscillator will indeed oscillate if the stages have very high gain. In practice, a ring with only two MOS inverters will not oscillate unless special effort is made in shaping the phase of the open loop transfer function[6]. Finally, Figure 2-4(c) shows that a system with three real poles will have sufficient phase shift to oscillate even for low loop gain.

To sumarize, for a ring oscillator with more than two stages and assuming that the Barkhausen criteria is met, the open loop transfer function, $H(j\omega)$, can be modeled by:

$$H(j\omega) = \frac{H_o^n}{\left(1 + \frac{j\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right)^n}, \qquad (2\text{-}12)$$

where the RHP feedforward zeros have been neglected. This approximation is valid as long as the number of stages is small, because for a small number of stages, the oscillator free runs at a frequency close to ω_p. To illustrate the consequences of (2-9), Table 2-1 shows the required voltage gain per stage and

6. It should be noted that a 2-stage oscillator can be easily implemented using bipolar technology [Maligeorgos00].

n	H_0	ω_p
3	2.00	0.58 ω_N
4	1.41	ω_N
5	1.24	1.38 ω_N

Table 2-1: Gain and free-running frequency for ring oscillators with 3, 4 and 5 stages..

free-running frequency as a function of number of stages for ring oscillators with 3, 4, and 5 stages. We observe that as the number of stages increases, the gain per stage required to meet the oscillation condition decreases. We note that for three or more stages, the contribution to C_L from the Miller-multiplied overlap capacitance is minimized as the voltage gain is close to unity. Moreover, the pole frequency ω_p does not necessarily coincide with the free-running frequency ω_0. In fact, ω_p coincides with ω_0 only for a 4-stage oscillator.

As illustrated conceptually in Figure 2-4(b), an oscillator with an even number of stages will require an additional inversion around the loop. Given our inverter model of Figure 2-3(b), it is not clear how this "extra" inversion can be accomplished. In practice, ring oscillators using an even number of stages are implemented using differential topologies. Figure 2-5 shows a 4-stage differential ring oscillator where the additional inversion around the loop is achieved by swaping the output wires. Equations (2-2) through (2-9) still apply, where g_m is the transconductance of the differential pair (M1, M2). In this case, each stage contributes 45 degrees of phase shift at ω_0. This property allows the 4-stage differential ring oscillator to be used as a source of quadrature signals[7].

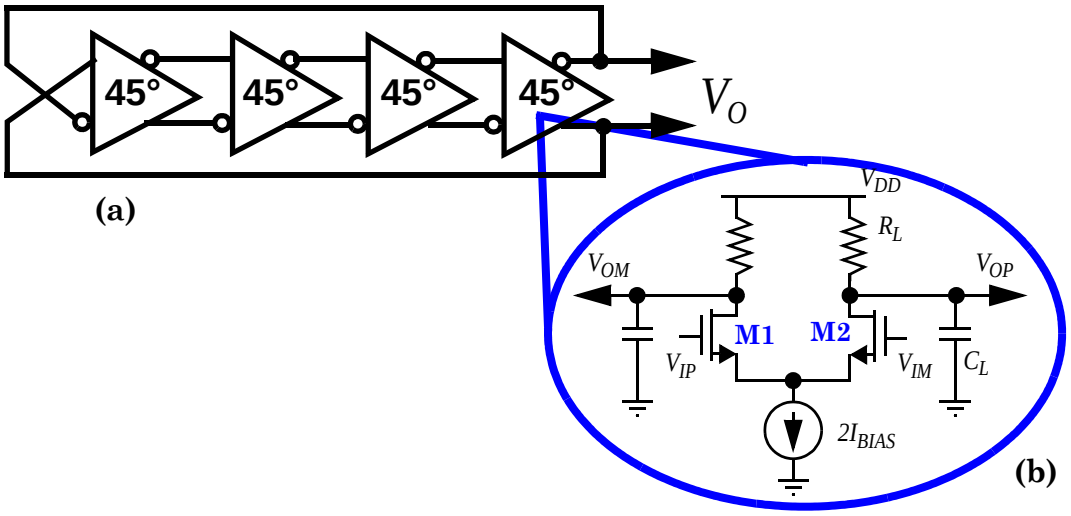

Figure 2-5 Differential ring oscillator model: (a) block diagram for 4-stage differential ring oscillator; (b) simplified circuit diagram for a differential inverter

Quadrature oscillators are of particular importance given that high quality, precision quadrature signal sources are essential for advanced image-reject radio architectures as well as clock and data recovery applications. To be fair, four-stage ring oscillators have some serious limitations when used to generate quadrature signals due to phase offsets caused by device mismatch among the stages. However, a number of quadrature generation techniques are available to overcome these limitations. Furthermore, a technique that minimize the deviation from perfect quadrature will be described in Chapter 5 when we discuss the injection-locked loop.

2.1.2 Voltage-Controlled Ring Oscillators

Finally, given the sensitivity of the system poles to variations in process, supply voltage, and temperature (PVT), a frequency stabilizing mechanism is required for frequency synthesis and clock generation applications. This is typically achieved using an external feedback control loop such as a phase-locked

7. Quadrature signals of the same frequency are separated in phase by 90° ($\pi/2$ radians) which is one-quarter of their period. In the context of communication circuits, quadrature signals are usually labelled “I” and “Q” to differentiate among the *in-phase* and *quadrature* components respectively.

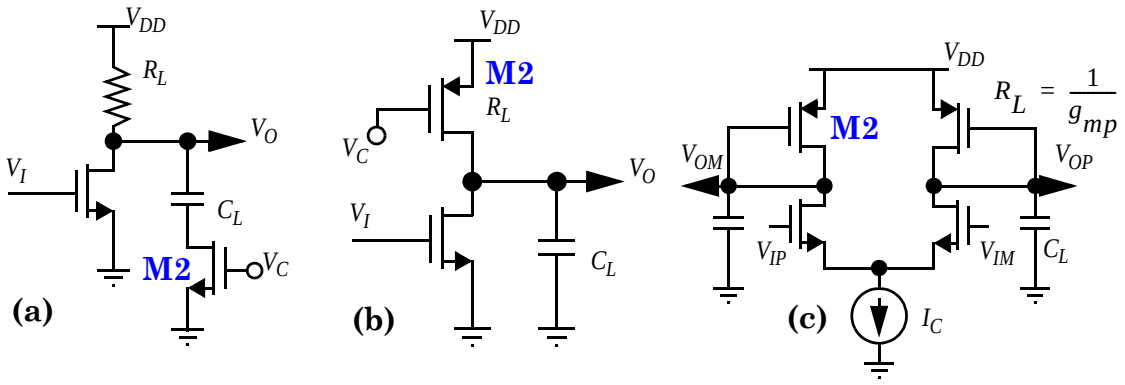

Figure 2-6 Voltage control of CMOS ring oscillator: (a) capacitive tuning; (b) triode load tuning; (c) diode load tuning

loop (PLL). In this case, the ring oscillator requires a frequency adjustment scheme controlled by either a voltage signal (i.e., a voltage-controlled oscillator, or VCO) or a current signal (i.e., a current-controlled oscillator, or CCO).

Control of the oscillation frequency can be achieved simply by changing the output pole time constant by varying either the load capacitance C_L or the output resistance R_L of the inverter stages. Figure 2-6 shows three examples of how this may be accomplished. In Figure 2-6(a), the output load capacitance C_L is varied using triode transistor M2. The amount of capacitance to ground "seen" by the output node is affected by the control voltage V_C. Linear capacitors (e.g., MIM[8], or dual-poly) should be used to minimize sensitivity to power supply variations. Finally, bottom plate and drain difussion parasitics establish a lower bound on the shift in capacitance available with this method. A modification of this technique may also be used to perform coarse frequency adjustment, by using a bank of capacitors controlled by MOS switches [Huang97].

8. Metal-insulator-metal (MIM) capacitors have low voltage coefficients, good matching, and small parasitics along with high reliability and low defect densities. With their high linearity and dynamic range, MIM capacitors are very useful in many types of RFICs.

In Figure 2-6(a), the output load R_L resistance is varied by adjusting the triode load transistor M2. This method is more complicated in that it requires a bias voltage for the PMOS load that guarantees operation in the triode region. Moreover, triode loads are inherently nonlinear, resulting in behavior that deviates from what is predicted by our simple LTI model. An undesirable side effect is that varying R_L also affects the DC gain of the inverter, thus special attention must be paid to guarantee that there is always sufficient gain to sustain oscillations. Finally, the output resistance of a diode-connected load transistor (M2) is inversely proportional to its transconductance which, in turn, is set by the bias current shown in the example of Figure 2-6(c). In this case, varying the tail bias current can be used to control the frequency of oscillation, thus implementing a current-controlled oscillator (CCO). A symmetric load topology that combines diode-connected and triode load transistors is described in more detail in Section 3.2.3 [Maneatis96].

It should be noted that in all cases above, the large signal behavior will deviate from what is predicted by the LTI model due to device nonlinearities. For large signal swings, the variation of the system time constants (i.e. poles and zeros) with the output voltage will become apparent. In this case, the oscillator circuits may be described more accurately by the nonlinear models discussed in Section 2.2.

2.2 Injection-locking Theory

The conventional definition of an electrical oscillator is that of an autonomous device that generates an alternating periodic current *without* requiring any external AC excitation. Now we would like to describe what happens when we lift that restriction and consider the behavior of an oscillator that is excited

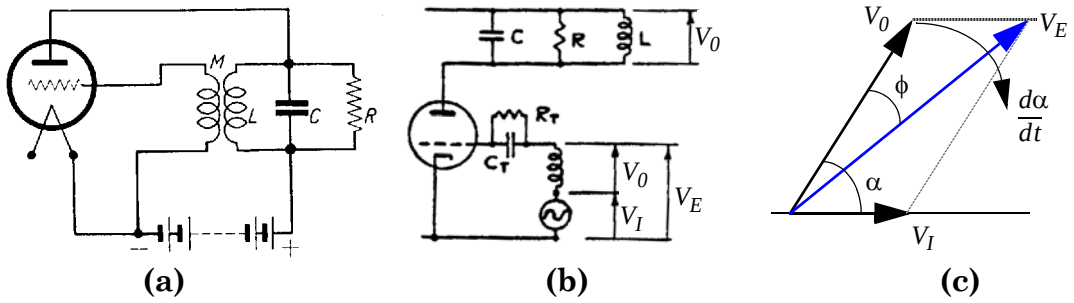

Figure 2-7 Triode oscillator circuits: (a) van der Pol; (b) Adler; (c) Adler's oscillator phasor diagram.

by an external signal.

Perhaps the first recorded demonstration of frequency entrainment[9] was made by Christiaan Huygens[10] in 1665, when he observed that two pendulum clocks hung on the same wall would eventually swing at exactly the same frequency and 180 degrees out of phase. When one pendulum was disturbed, the antiphase state was restored within half an hour and sustained indefinitely. He found that synchronization did not occur when the clocks were isolated from each other and deduced that the interaction came from mechanical coupling through the common frame supporting the clocks. These observations inspired the study of coupled oscillators in many fields. Furthermore, the onset of synchronization is a fundamental problem of nonlinear dynamics and one which has been vigorously pursued for many years.

2.2.1 Van der Pol's Nonlinear Theory of Oscillators

The process by which an oscillator tracks a weak injected signal of similar frequency, was first studied in detail by Balthasar van der Pol[11] in the 1920s. While investigating vacuum tube circuits, he found that when they are

9. Another term for synchronization of coupled oscillators or injection-locking.
10. Dutch astronomer and mathematician Christiaan Huygens (1629-1695) patented the first pendulum clock in 1656. He is also known for his support of the wave theory of light which he used to deduce the laws of reflection and refraction.

driven with a signal whose frequency is near that of the limit cycle, the resulting periodic response shifts its frequency to that of the driving signal. That is to say, the circuit becomes *entrained*[12] to the driving signal. In his seminal paper [vanderPol34], van der Pol derived the non-linear differential equations required for the analysis of resonant and relaxation triode oscillators. The *van der Pol equation* for the *RLC* triode[13] oscillator (Figure 2-7a) is given by:

$$\frac{d^2v}{dt} - \alpha(1 - v^2)\frac{dv}{dt} + \omega_0^2 \cdot v = \omega_I^2 V_I \sin\omega_I t \qquad (2\text{-}13)$$

$$\varepsilon = \frac{\alpha}{\omega_0} \ll 1 \text{ ; sinusoidal oscillator} \qquad (2\text{-}14)$$

$$\varepsilon = \frac{\alpha}{\omega_0} \gg 1 \text{ ; relaxation oscillator,} \qquad (2\text{-}15)$$

where ω_0 is the free-running frequency of the oscillator and ω_I is the frequency of an externally applied signal of amplitude V_I. For this derivation, the triode's nonlinear relationship between the plate current and the grid voltage (with a constant plate voltage) is approximated by a third order polynomial. Fortunately, this equation also describes the behavior of a MOSFET oscillator.

We begin by considering the behavior of the homogeneous equation, where there is no external injected signal ($V_I = 0$) and $\varepsilon = 0$. In this case, Equation (2-13) reduces to that of a harmonic oscillator and all solutions are periodic

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11. Dutch physicist Balthasar van der Pol (1889 - 1959) studied experimental physics with J. A. Fleming and Sir J. J. Thompson in England. He initiated the field of modern experimental dynamics during the 1920s and 1930s. He built a number of electronic circuit models of the human heart to study the range of stability of heart dynamics. His investigations with adding an external driving signal were analogous to the situation in which a real heart is driven by a pacemaker. He was interested in finding out how to stabilize a heart's arrhythmias. This is probably the first known account of using injection-locking in a medical application.

12. Entrainment means that the oscillation waveform is asymptoticallv periodic with a period which is an integer multiple of the period of the driving signal. It is synonymous with injection-locking.

13. In 1907, Lee de Forest (1873-1961) invented the triode, a thermionic vacuum tube with three electrodes: cathode, plate, and grid. Varying the voltage on the grid controls the flow of electrons from the cathode to the plate.

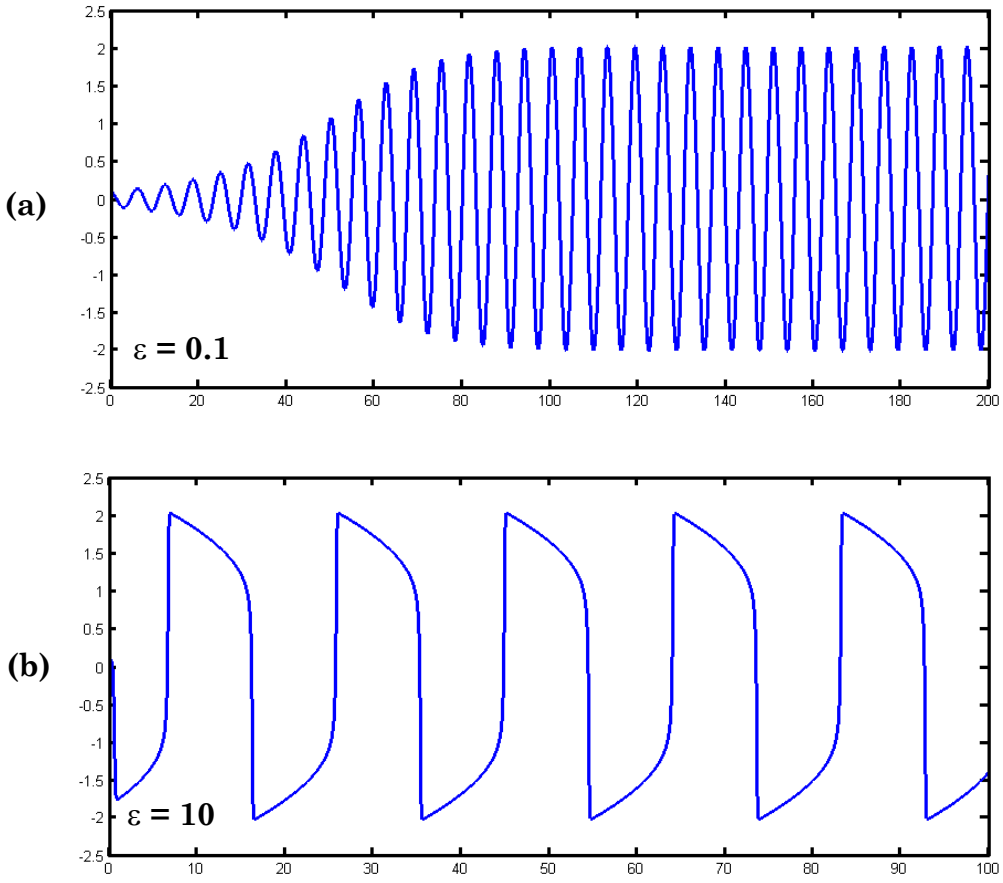

Figure 2-8 Van der Pol oscillator waveforms for ω_0 =1: (a) sinusoidal oscillator; (b) relaxation oscillator with $v(t) = a_1 \cos t + a_2 \sin t$ [Guckenheimer80].

A more interesting result is obtained when $0 < \varepsilon \ll 1$ (2-14). Given a small positive constant ε, the system will be unstable, and therefore prone to oscillation. Consider again the case where there is no injected signal and suppose that due to thermal noise or a power-on transient, a small signal is present in the system. For small amplitudes, the circuit has a negative resistance that contributes to an exponential increase in the oscillatory envelope. As the amplitude increases, the $v^2 \frac{dv}{dt}$ term increases slowly and the magnitude of the negative resistance decreases. At some point the resistance changes sign, thus

dampening the growth in the envelope until a final stable amplitude is reached. Figure 2-8(a) shows an example where $\varepsilon = 0.1$. This change from a negative resistance towards a positive resistance and the resulting amplitude stabilization is due to the bend in the gain characteristic of the amplifier and therefore cannot be predicted by the LTI model of the simple harmonic oscillator.

First, let's introduce an external signal injected at frequency ω_1 near ω_0. It was demonstrated by van der Pol that the oscillator frequency will be *synchronized* or "*locked*" to that of the injected signal in a small region near resonance[14]. The range of frequencies over which synchronization occurs, i.e., the *locking range,* is proportional to the injected signal amplitude.

Now, consider the condition where $\varepsilon \gg 1$, again, without injection (Equation 2-15); this case describes the behavior of a *relaxation oscillator*[15]. This mode is interesting because, in the large signal regime, the ring oscillator also exhibits a relaxation behavior that can be described by Equation (2-13). Figure 2-8(b) shows an example where $\varepsilon = 10$. We observe that the waveform, although still periodic, has the characteristics of a repeating discharge phenomenon with period given by a relaxation time constant proportional to RC or L/R. Moreover, the oscillation period is greater than what is predicted by an LTI model. The final amplitude is reached sooner (within one cycle), and the waveform is rich in harmonics. Frequency synchronization is also predicted by Equation (2-13) for the relaxation oscillator. However, the locking range is considerably wider than that of the sinusoidal oscillator. Furthermore,

14. The injected signal not only entrains the oscillator frequency, but can also increase greatly the oscillation amplitude. This property has been exploited successfully in injection-locked narrowband amplifiers.

15. An astable multivibrator is a good example of a relaxation oscillator whose period is controlled by the charging and discharging of a capacitor. The relaxation phenomenon is also found in nature, for instance, in the generation of a heartbeat and in neural signals.

synchronization to subharmonics of the injected signal is also observed[16]. A model that describes this harmonic locking mechanism in ring oscillators is discussed in Chapter 4.

It is now evident that the LTI theory of Section 2.1 is inadequate to accurately describe the behavior of a relaxation oscillator and its synchronization mechanism. Moreover, it is the presence of a nonlinear element in the system that allows synchronization to occur. However, because a formal analytical solution does not exist for the van der Pol equation, the LTI model is still useful for the design insight that it provides.

2.2.2 Adler's Study of Injection Locking Phenomena

A more intuitive treatment of injection locking is given in a classic article by Adler[17], who studied the synchronization mechanism [Adler46]. Suppose we inject a weak signal close to the free-running frequency of a triode oscillator identical to van der Pol's where $\varepsilon \ll 1$ (Figure 2-7b). Adler derives the following differential equation for the oscillator phase as a function of time:

$$\frac{d\alpha}{dt} = -\frac{V_I}{V_0} \cdot \frac{1}{S} \sin\alpha + \Delta\omega_0 \tag{2-16}$$

$$S = \frac{d\phi}{d\omega}, \tag{2-17}$$

where, V_I and V_0 are the strengths of the external signal and oscillator respectively and $\Delta\omega_0 = \omega_0 - \omega_I$ is the frequency difference between the free running oscillation and the injected signal. Adler's phasor diagram of Figure 2-7c shows the relationships among the other variables: α is the phase difference

16. Frequency demultiplication (i.e., frequency division) using relaxation oscillators was verified experimentally for ratios of up to 200:1.

17. Dr. Adler is best known as the "Father of the TV Remote Control." He developed the ultrasonic remote control for TV sets introduced by Zenith in 1956.

between the two signals, $\frac{d\alpha}{dt}$ represents the angular beat frequency relative to the external signal, and S is the slope of the phase response of the tank circuit linearized around ω_0. Injection locking implies that $\frac{d\alpha}{dt} = 0$ and therefore the solution to Equation (2-16) becomes:

$$\sin\alpha = \frac{V_0}{V_I} \cdot S \cdot \Delta\omega_0. \tag{2-18}$$

This leads to an expression for the steady state phase between the oscillator and the impressed signal:

$$\alpha = \operatorname{asin}\left(\frac{V_0}{V_I} \cdot S \cdot \Delta\omega_0\right) \cong \frac{V_0}{V_I} \cdot S \cdot \Delta\omega_0 \,, \tag{2-19}$$

which is valid for injection close to the oscillator's free-running frequency (i.e., small $\Delta\omega_0$). This function is antisymmetric around ω_0, and the phase approaches $\pm\pi$ as the frequency offset approaches the limits of the locking range. Finally, because sin α must be in the range [-1, 1], Equation (2-19) implies that:

$$\left|\Delta\omega_{max}\right| < \frac{V_I}{V_0} \cdot \frac{1}{S} \,. \tag{2-20}$$

This expression gives the locking range of the oscillator, where $\Delta\omega_{max}$ is the maximum value of $\Delta\omega_0$ for which locking may occur. Note that the locking range depends on the strength of the injected signal relative to the oscillator's amplitude, and is inversely proportional to the slope of the phase characteristic of the resonant network.

For the triode oscillator, S can be approximated using:

$$\tan\phi = \frac{2Q}{\omega_0} \cdot \Delta\omega \cong \phi \text{ , for small angles} \tag{2-21}$$

$$S = \frac{d\phi}{d\omega} = \frac{2Q}{\omega_0} \tag{2-22}$$

$$\left|\frac{\Delta\omega_0}{\omega_0}\right| < \frac{V_I}{V_0} \cdot \frac{1}{2Q} \,, \tag{2-23}$$

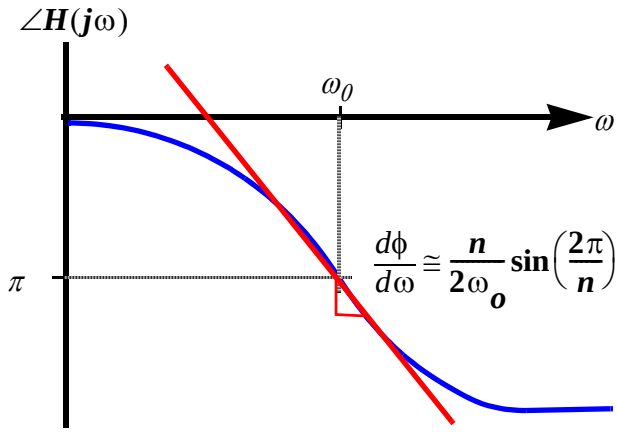

Figure 2-9 Open-loop phase transfer characteristic of n-stage ring oscillator, *H(jω)*.

where $\Delta\omega = \omega - \omega_0$, and Q is the quality factor of the tank circuit. This leads to the classic form of Adler's equation (2-23) that reveals the inverse relationship between the Q-factor of an LC oscillator and its locking range. Simply put, to achieve maximum locking range, use a low-Q network and a relatively large injected signal.

Similarly, following Adler's method, we derive an approximate analytical expression for the locking range of a ring oscillator using the LTI filter model derived in Section 2.1. Consider the linearized phase response of the n-stage $H(j\omega)$ filter (Figure 2-9) described by Equation (2-12):

$$\phi = \pi + \angle H(j\omega) = \pi + n\,\mathrm{atan}\left(\frac{\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right) \tag{2-24}$$

$$\phi \cong \pi + S \cdot \Delta\omega \tag{2-25}$$

$$S = \frac{n}{2\omega_0}\sin\left(\frac{2\pi}{n}\right). \tag{2-26}$$

Substituting Equations (2-26) into (2-26), we arrive at

$$\left|\frac{\Delta\omega_0}{\omega_0}\right| < \frac{V_I}{V_0} \cdot \frac{2}{n \cdot \sin\left(\frac{2\pi}{n}\right)} \tag{2-27}$$

which, as expected, also shows that the locking range is proportional to the

relative strength of the injected signal. Futhermore, the locking range is inversely proportional to the number of stages n: As the number of stages increases, the slope of the phase transfer function $H(j\omega)$ becomes "steeper" thus reducing the achievable locking range. For a large number of stages, we get:

$$\lim_{n\to\infty} \frac{V_I}{V_0} \cdot \frac{2}{n \cdot \sin\left(\frac{2\pi}{n}\right)} = \frac{V_I}{V_0} \cdot \frac{1}{\pi} . \tag{2-28}$$

In conclusion, the locking range of the ring oscillator can be maximized by increasing the injected signal strength and minimizing the number of stages.

Aside from the locking range, it is also important to understand the transient response of the injection-locked oscillator, as it reveals much about its phase noise filtering properties. Adler also described the transient response of the oscillator phase for weak injection[18]. Suppose that the output frequency is close to ω_0 ($\Delta\omega_0 \cong 0$). For a small phase step α, equation (2-16) reduces to the first-order differential equation

$$\frac{d\alpha}{dt} = -\frac{V_I}{V_0} \cdot \frac{1}{S}\sin\alpha \cong -\frac{V_I}{V_0} \cdot \frac{1}{S}\alpha \tag{2-29}$$

with solution of the form $\alpha = k \cdot e^{-t/\tau}$ (2-30)

where $$\tau = \frac{V_0}{V_I} \cdot S = \frac{1}{\Delta\omega_{max}} . \tag{2-31}$$

We can observe from this equation that the same parameters affect both the locking range and the time constant τ where the locking range is approximately the 3-dB bandwidth of the first-order system response. Therefore, maximizing the locking range also results in the best transient performance. Moreover, the oscillator is able to track any phase noise of the injected source within its locking range bandwidth $\Delta\omega_{max}$.

18. "[...] this means physically that the oscillator phase sinks toward that of the impressed signal, first approximately, and later accurately as a capacitor discharges into a resistor." [Adler46].

Further studies extending Adler's analysis of the dynamics of the locking process for both small signal and large signal injection can be found in [Paciorek65] and [Kurokawa73]. Kurokawa also studies the resulting stability and noise.

2.2.3 Harmonic Locking in Oscillators

Adler does not address harmonic locking directly. However, an extension of this mechanism for superharmonic injection is described in [Rategh99]. Rategh observes that the same nonlinearity that is responsible for limiting of the oscillation amplitude also produces intermodulation products[19] of ω_I and ω_0 that influence the synchronization mechanism.

First, suppose that Adler's oscillator operates at its natural frequency and that the $H(j\omega)$ filter suppresses frequencies far from ω_0. Further, if we assume that $\omega_I = N\omega_0$ then the only intermodulation terms not suppressed by the filter will have $mN \pm n = 1$ for some integers m and n, where $m\omega_I$ and $n\omega_0$ are the harmonics of the input and output frequencies, respectively. These intermodulation products introduce a phase shift that depends upon the strength of injection and the intermodulation Fourier coefficients, $K_{m,\, mN \pm 1}$. Adler's equation can then be modified as shown by [Rategh99]

$$\Delta\omega_N = \Delta\omega_{max}\left[\frac{H_o}{2V_I}\sum_{m=1}^{\infty} K_{m,\, mN \pm 1}\sin(m\alpha)\right] \tag{2-32}$$

$$\Delta\omega_N = \frac{\omega_I}{N} - \omega_0\,, \tag{2-33}$$

where $\Delta\omega_{max}$ is Adler's locking range as given by Equation (2-20).

19. Intermodulation refers to the production of frequencies corresponding to the sums and differences of integral multiples of the fundamentals and harmonics.

Second, observe that to maintain synchronization at higher harmonic ratios N requires the presence of stronger intermodulation products for the locking conditions to be satisfied. This confirms van der Pol's observation that an LC oscillator driven into the relaxation regime (i.e. rich in harmonics) will have greater locking range for large harmonic ratios. On the flip side, undesirable harmonic locking is more likely in relaxation oscillators even when implemented with high-Q tuned circuits.

Third, even though Rategh makes a distinction beween them, both the Miller and the injection-locked dividers are special cases of a harmonically-locked feedback system since the locking mechanism and equations that describe their behavior are identical. In Chapter 4, we present a generalized mixer-based model based on Miller's regenerative frequency divider where we describe both the Miller and harmonic-locked dividers in more detail. A more general model is presented in [Verma03].

Finally, the next section briefly surveys the literature and outlines the historical development of the injection-locked ring oscillator frequency divider.

2.3 Historical Development of Injection-locked Ring Oscillator Frequency Dividers

Now that we have a rudimentary analytical understanding of the theory of operation of ring oscillators and the injection-locking mechanism we will briefly discuss the historical events that led to the development of the injection-locked ring oscillator frequency divider.

Injection-locked oscillators have been used to perform a wide range of tasks, including amplification with limiting [Carnahan44], [Smith91], frequency multiplication [Fukatsu69], frequency and phase modulation [Ruthroff68],

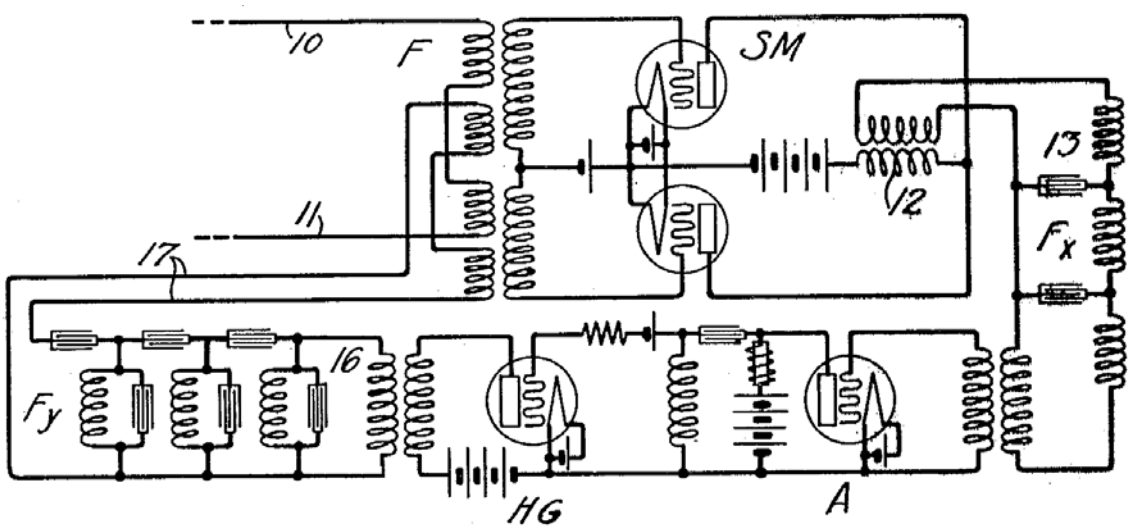

Figure 2-10 Horton's Regenerative Frequency Divider (circa 1922)

and phase shifting. In fact, an entire receiver can be built solely with the use of injection-locked oscillators [Edmonson92].

The concept of regenerative[20] frequency division can be traced back to an invention by J. W. Horton [Horton28]. In 1922, while working at Western Electric, he developed a frequency divider for carrier distribution in multi-channel telephony. Figure 2-10 shows a simplified schematic of this early device where a balanced modulator *SM* mixes frequencies *F* and *Fy* whose products are filtered by *13*, the output of which is *Fx*. This signal is then amplified by *A* and excites harmonic generator *HG*. Filter *16* then selects a harmonic that becomes *Fy*, thus closing the loop. At the time, however, due to its complex implementation, this circuit did not achieve widespread adoption, but it formed the basis for Miller's later work on regenerative frequency dividers.

In 1927 Koga presented a "frequency transformer" which is one of the earliest known accounts of a harmonically-locked oscillator used explicitly as a

20. Regeneration is the process of returning energy back into the system during a portion of the device's cycle. This is an early term used to describe systems with positive feedback.

frequency divider [Koga27]. Koga describes in detail experiments that demonstrated the operation of a triode-based Hartley oscillator being "synchronized" to an external source at division ratios of 2 through 8. Koga experimented by varying the strength of the injected signal and showed a decrease in locking range as a function of the harmonic ratio.

In 1930 Groszkowski described the phenomenon of frequency division as being *contra natura* [Groszkowski30]. He presented an approximate analysis based on the analogy of two pendulums: a longer one excited by a shorter one loosely coupled by means of a thread. He also presented experimental results for an injection-locked frequency divider based on a triode oscillator.

Even though both Koga and Groszkowski had a rudimentary understanding of the mechanism responsible for injection-locking, it was van der Pol with his non-linear theory of oscillators [vanderPol34] who established the basis for a more rigorous analysis of this phenomenon. Investigating vacuum tube circuits, he found that a triode oscillator can become synchronized to an injected signal (Section 2.2.1). He also observed synchronization to harmonics of the injected signal. Numerical solutions to van der Pol's relaxation oscillator equations using a differential-analizer were presented by Herr in 1939 [Herr39]. This is the first known "computer" simulation of the injection-locking phenomenom.

According to Sterky , harmonic locking was already used in frequency multipliers for commercially available multi-channel carrier telephony products as early as 1929 [Sterky37]. However, it was not until 1939, when R. L. Miller published an article on the theory and applications of the principle of regenerative modulation, that the regenerative divider (Figure 2-11) became widely known [Miller39]. It is interesting to note that Miller's divider does not

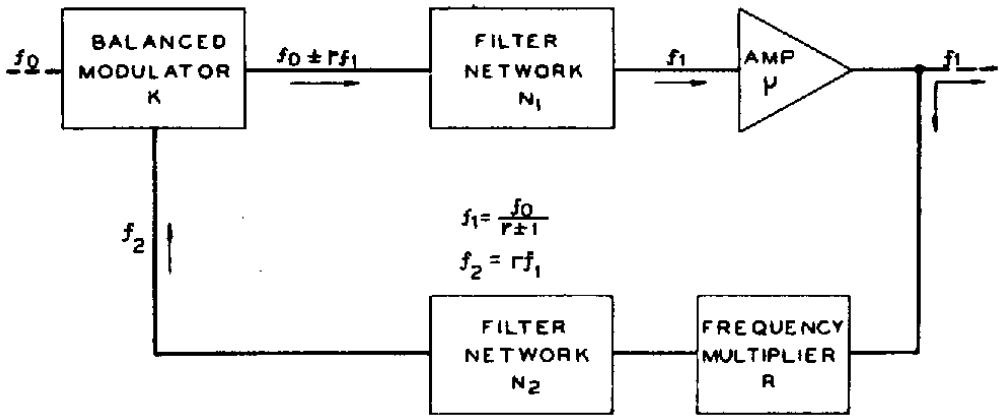

Figure 2-11 Miller's schematic diagram of regenerative modulator

produce an output in the absence of an injected signal, while a harmonically-locked oscillator oscillates freely even without signal injection.

Until recently most authors have made a distinction between regenerative dividers that use explicit mixers and filters in a feedback loop and harmonically-locked oscillators. Miller himself emphasized the advantages of the former as if they were distinct, unrelated mechanisms. However, we will show in Chapter 4 that any harmonically-locked oscillator can be described using a generalized mixer-based model similar to Miller's, since the synchronization mechanisms are identical.

With the advent of the monolithic microwave integrated circuit (MMIC), integrated injection-locked dividers became more commonly used in applications where the frequency of operation is beyond what can be achieved with flip-flop based circuits. Efforts at frequencies beyond 5 GHz were reported using injection-locking to implement divide-by-2 prescalers in CMOS [Rategh00], and Si-BJT technologies [Derksen88], [Ichino89]. This principle has also found common use at millimeter-wave frequencies in GaAs [Maligeorgos00] and SiGe technologies [Kudszus00a].

It was not until the recent proliferation of high frequency digital ICs that injection-locked ring oscillator structures have become a subject of more intense study. Digital dividers using current-mode logic (CML) at very high frequencies, where signal amplitudes are small, have been known to self-oscillate [Nishi90],[Kado90]. In this regime, these circuits behave more like ring oscillators [Knapp00a]. A more explicit use of the ring oscillator structure was made by [Madden96] who presented a 75-GHz 2-stage ring divider in InP technology and by [Teetzel92] who showed a 1.6-GHz frequency divider implemented in GaAs.[Long96] also discussed an injection-locked ring oscillator standard cell in CMOS using an explicit mixer in the feedback path.

Maneatis and Horowitz [Maneatis93] used an array of injection-locked oscillators based on a series of coupled CMOS ring oscillators to generate multiple clocks with precise spacing. To couple rings together, they used a dual-input buffer where both the ring and coupling input transition times determine when the output transition will occur, i.e., early coupling inputs reduce the buffer delay, while late coupling inputs increase the buffer delay. In this work, even though there is no *external* signal injection, the injection-locking phenomenom was exploited to coerce precise phase offsets among multiple ring oscillators. This paper also presents a rudimentary linear model that defines the boundary conditions for locking.

A more detailed discussion of injection-locked oscillator arrays (in the context of active antenna beamforming for millimiter wave radar) can be found in [York98].

The first explicit use of a CMOS injection-locked ring oscillator for low-power frequency division was reported by Aebischer et al.in 1997 [Aebischer97]. A 5-stage current-starved ring oscillator was used to implement

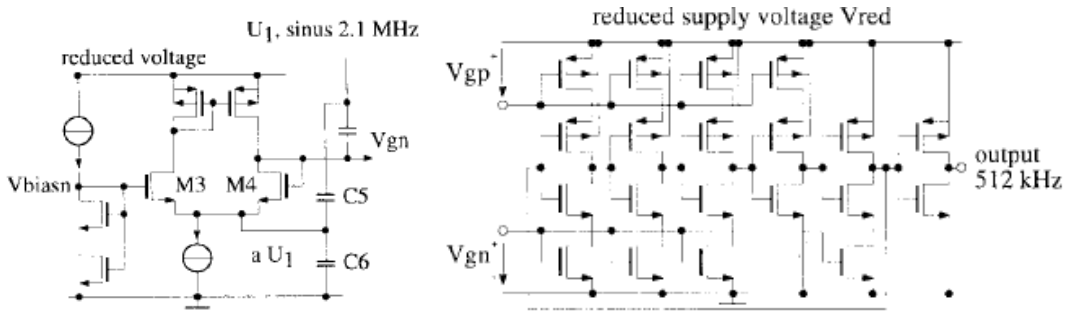

Figure 2-12 CMOS ring oscillator modulo-4 frequency divider [Aebischer97]

a 2.1-MHz modulo-4 frequency divider. Current consumption was in the order of 300nA. As shown in Figure 2-12, the input signal is capacitively coupled to the Vgp and Vgn nodes. These nodes bias the inverters in the subthreshold regime using an "interface circuit" that compensates for the amplitude of the injected AC signal. This dependence of the injected signal amplitude on the oscillator's bias is discussed in more detail in Chapter 4. The ring oscillator frequency divider in CMOS was revisited by [Betancourt01] and [Chen02] for RFIC applications.

The last decade has also seen a resurgence of interest in the theoretical basis of injection-locked oscillators. A theoretical analysis of phase noise in regenerative dividers is presented by Rubiola, et al. in [Groslambert91] and [Rubiola92]. An analysis of the locking range and stability is given by [Harrison89], [Derksen91], and [Ciubotaru94]. More recently, phase noise in injection-locked oscillators was studied by [Rategh99], [Betancourt01], [Verma03], [Razavi04], and [Mazzanti04]. In particular, Verma's use of the Hajimiri phase noise theory is described in Section 4.2.3.

Uzunoglu and White's paper [Uzunoglu85] described the basis for what they called "synchronous oscillators." They used Adler's theory to analyze a discrete implementation of an injection-locked Colpitts oscillator, and describe its

application to carrier and clock recovery networks in QPSK modems. Their work along with [Harrison89] established the foundation for Rategh's later work [Rategh99]. In 1989 they introduced the coherent phase-locked synchronous oscillator (CPSO), which adds a phase tracking loop to the synchronous oscillator to extend its locking range [Uzunoglu89]. Extending the locking range with a phase tracking loop is described further in Chapter 5. In 1999, Badets et al., presented an integrated synchronous oscillator in a 0.8-μm BiCMOS process [Badets99a], [Badets99b].

Finally, a quadrature-phase generator in silicon bipolar technology is presented in [Maligeorgos00] and later reimplemented in SiGe by Chung and Long [Chung04]. The structure is similar to that of a 2-stage ring oscillator with quadrature injection using two mixers. Although the authors claim a quadrature error of less than 1°, this circuit requires manual adjustment of the mixer bias currents in order to null the quadrature error due to device mismatches and the injection mechanism itself. Quadrature-phase generation will be discussed in more detail in Chapter 5.

2.4 Summary

In this chapter, a simple ring oscillator theory is presented, along with an introduction to modeling of injection-locked processes based on the work by van der Pol and Adler. The historical development and applications of injection-locking to ring oscillators is also discussed.

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Chapter 3

Voltage-controlled Ring Oscillators

In this chapter, we describe new design insights, methods, and tools which shorten the design time for low-power integrated high-frequency ring oscillators. First, we present a methodology that uses a new phase noise model to trade-off phase noise and power dissipation in the design of ring oscillators suitable for frequency synthesis. Second, we compare the phase noise performance of three buffer stages using clamped, symmetric and cross-coupled loads, respectively. Finally, we propose a cross-coupled buffer topology that achieves lower phase noise by exploiting symmetry. This topology achieves a 95% reduction in the $1/f^3$ corner frequency of the phase noise characteristic.

3.1 Introduction

Frequency synthesizers provide the precise reference frequencies for modulation and demodulation of RF signals. Traditionally, frequency synthesizers have been implemented using phase-locked loops (PLL). As described in Chapter 1, the major sources of power dissipation in a PLL are the voltage-controlled oscillator (VCO) and the frequency divider.

Ring-based voltage-controlled oscillators are well-suited for integration since they require no external components. While their intrinsic phase noise is relatively high compared to that of LC oscillators, the dominant noise source is often due to the power supply. However, phase noise is particularly important in RF systems as it can lead to increased bit error rates (BERs) in digital communication systems, contamination of adjacent frequency channels, and receiver desensitization due to reciprocal mixing where out-of-band signals are translated into the IF [Crawford94] (See Section “3.2.2” on page 46).

A voltage-controlled ring oscillator’s power dissipation is determined by the frequency of operation and the phase noise performance required. Power dissipation at a given frequency cannot be made arbitrarily small, as it is constrained by the choice of technology, and by the system’s phase noise requirements. The next section presents a design methodology for differential ring oscillators that takes into consideration the tradeoff between power dissipation and phase noise.

3.2 Ring Oscillator Design

Analysis and design of ring oscillators form the core of this chapter. Ring oscillators are probably the simplest type of oscillator used in RFIC design. They are routinely incorporated on-chip for quality monitoring of the semiconductor manufacturing process. A simple LTI theory that describes the startup condition for ring oscillators was already discussed (See Section “2.1” on page 12). In this section we will focus on practical design issues of differential ring oscillators, their power vs. operating frequency, and power vs. phase noise performance trade-offs.

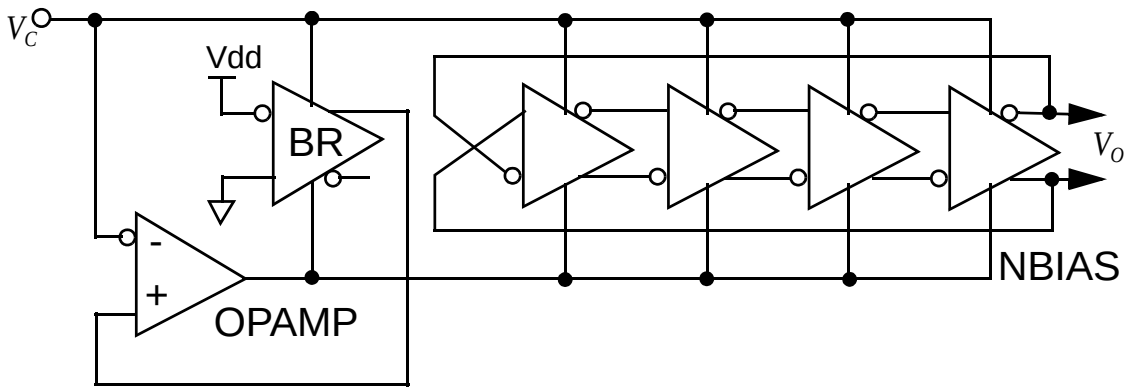

Figure 3-1 Block diagram of differential ring oscillator with replica-feedback biasing

3.2.1 Power vs. Frequency Trade-off

In this study, we consider a differential ring oscillator VCO topology (Figure 3-1) with replica-feedback biasing [Maneatis93]. The delay buffers are NMOS differential pairs with PMOS loads. The replica bias feedback ensures that the loads are always in their linear region by forcing the swing V_S to be the same as (V_{DD} - V_{CTL}). Frequency control is achieved by varying V_{CTL} which also changes the bias *Idd* of the buffer stages. For ring oscillators based on differential-pair buffer stages, the total power dissipation is given by

$$P = NI_{dd}V_{dd}, \tag{3-1}$$

where N is the number of stages, *Idd* is the tail current of the differential pair, and *Vdd* is the supply voltage. The frequency can be approximated by

$$f \approx \frac{I_{dd}}{2NC_L V_S}, \tag{3-2}$$

where C_L is the total load capacitance and V_S is the maximum single-ended voltage swing at the output of each stage. Figure 3-2 shows the power dissipation vs. free-running frequency of the differential ring oscillator for different sizes of the differential-pair transistors in a 0.5μm CMOS process.

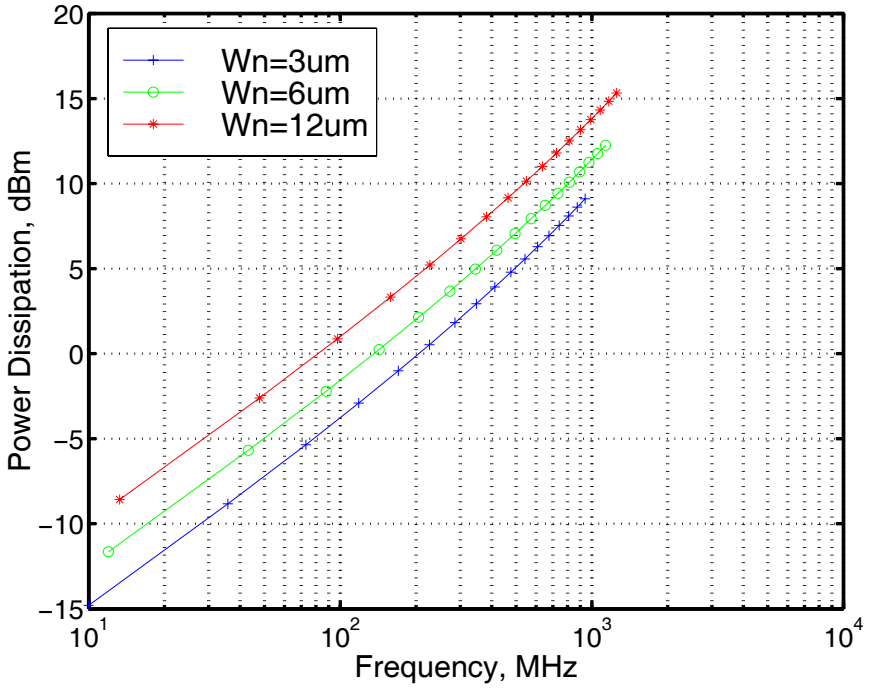

Figure 3-2 Power dissipation of differential ring oscillator for different device widths

3.2.2 Power vs. Phase Noise Trade-off

Before we delve deeper into this topic we need to define a metric for oscillator phase noise and establish why it is so important. Phase noise may be defined as rapid, short-term, random fluctuations in the phase of a wave caused by time-domain instabilities in an oscillator due to intrinsic device thermal and flicker noise. It is usually expressed as a ratio of single sideband power density reported in decibels relative to carrier power (dBc), normalized to a 1-Hz bandwidth (dBc/Hz) at a specified offset frequency from the carrier. It is given by $L(\Delta f) = 10 \cdot \log\{S_f(\Delta f)/2\}$ where $S_f(\Delta f)$ is the spectral density of phase fluctuations (Figure 3-3). Phase noise is particularly important in RF systems as it can lead to increased bit error rates (BERs) in digital communication systems, contamination of adjacent frequency channels, and receiver desensitization due to reciprocal mixing where out-of-band signals are translated into the IF [Crawford94].

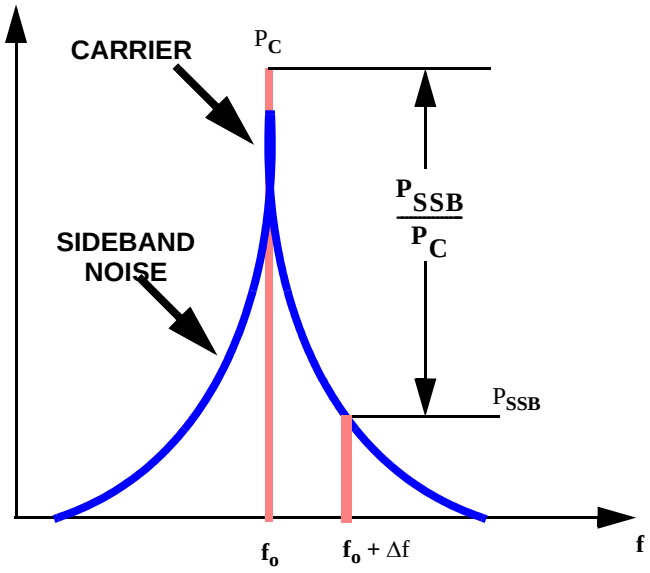

Figure 3-3 Definition of oscillator phase noise as a ratio of single-sideband noise power (P_{SSB}) to total carrier power (P_C) at a specific offset frequency Δf

For instance, in a typical digital communication system phase noise in the local oscillator can cause the signal constellation to rotate in a random fashion, thereby degrading the BER performance. Figure 3-4 shows the effects of noise on the constellation for a QPSK[1] modulated signal, where (a) shows the effect of additive white gaussian noise (AWGN), while (b) adds the effect of phase noise at the carrier frequency. The noise has been exaggerated for illustration purposes. Phase noise increases the probability of error in the detection of the signal by reducing the effective distance between the symbols.

Figure 3-5 shows an example of reciprocal mixing in a superheterodyne receiver. It shows a weak signal in the desired channel accompanied by a strong interferer in the adjacent channel. Any significant phase noise of the local oscillator at a frequency offset that coincides with the interferer will downconvert it down to the intermediate frequency (IF). The desired signal thus gets buried under the phase noise skirt of the adjacent interferer.

1. *Quadrature phase-shift keying* is a modulation technique that allows two bits per signaling element by using four different phase angles.

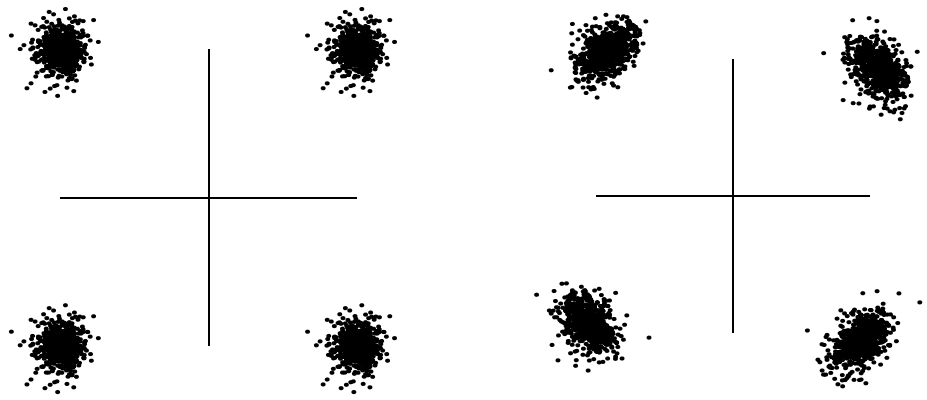

Figure 3-4 QPSK constellation: (a) with AWGN, (b) with AWGN and oscillator phase noise

The relevance of oscillator phase noise in frequency synthesizers is obvious when we examine the noise transfer function of a phase-locked loop (PLL). A PLL tracks the phase noise of the reference signal within its loop bandwidth. This relaxes the close-in phase noise requirements of the VCO, provided that the reference signal has better phase noise than the VCO. At frequencies beyond its bandwidth, the PLL cannot reject the VCO's phase noise. This is why VCO phase noise is usually specified at frequency offsets beyond the suppression range of the PLL.

The Hajimiri phase noise model [Haji98a,Haji98b,Haji98c] predicts the upconversion of thermal and *1/f* device noise into close-in phase noise. To illustrate this process, Figure 3-6 shows the effect of a noise source in a simple parallel LC tank oscillating circuit. We observe that a current impulse injected at the peak of the wave only changes the amplitude and has no effect on the phase, whereas injection at the zero-crossing causes a nonzero step change in the phase and has minimal effect on the amplitude. Moreover, the magnitude of the step is not only a function of the amplitude of noise injected but also of when in the cycle the injection occurs. This observation can be used to derive a time-variant expression for the impulse response of the oscillatory system.

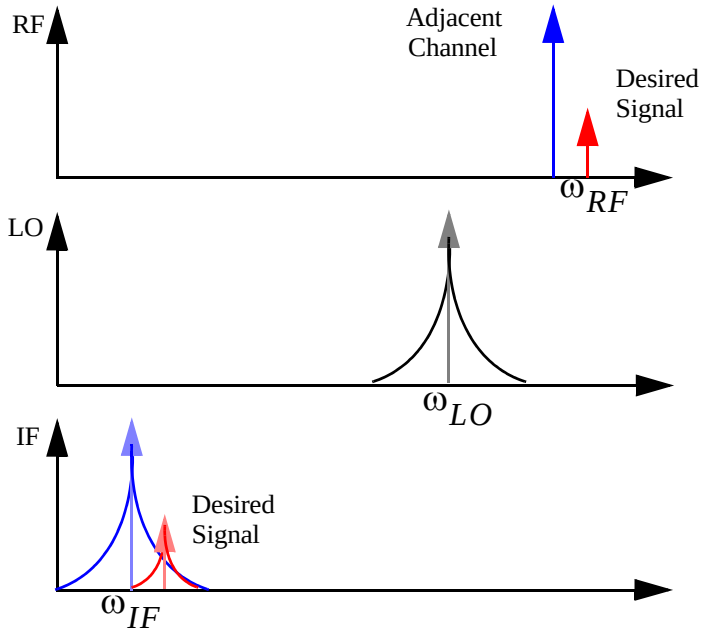

Figure 3-5 Receiver desensitization due to reciprocal mixing

For small injection amplitudes, Hajimiri has shown that the injected noise-to-phase noise transfer characteristic can be described by the following linear time-variant equation:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau)\ , \tag{3-3}$$

where h_ϕ is the unity impulse phase response, q_{max} is the maximum charge displacement in the tank, $u(t)$ is the unit step function, and $\Gamma(x)$ is the impulse sensitivity function (ISF) that describes the sensitivity of the oscillator to a unit impulse at any point in time. The ISF is also a function of the output waveform and it accounts for the time-variant sensitivity of the oscillator to its noise sources. It can be calculated directly from the oscillator's waveform and may be expressed by the Fourier series

$$\Gamma(\omega_0\tau) = c_o + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} \cos(n\omega_0\tau)d\tau\ , \tag{3-4}$$

where c_n are real value coefficients. We may use this equation along with the linear expression in (3-3) to calculate the output excess phase $\phi(t)$ for a small

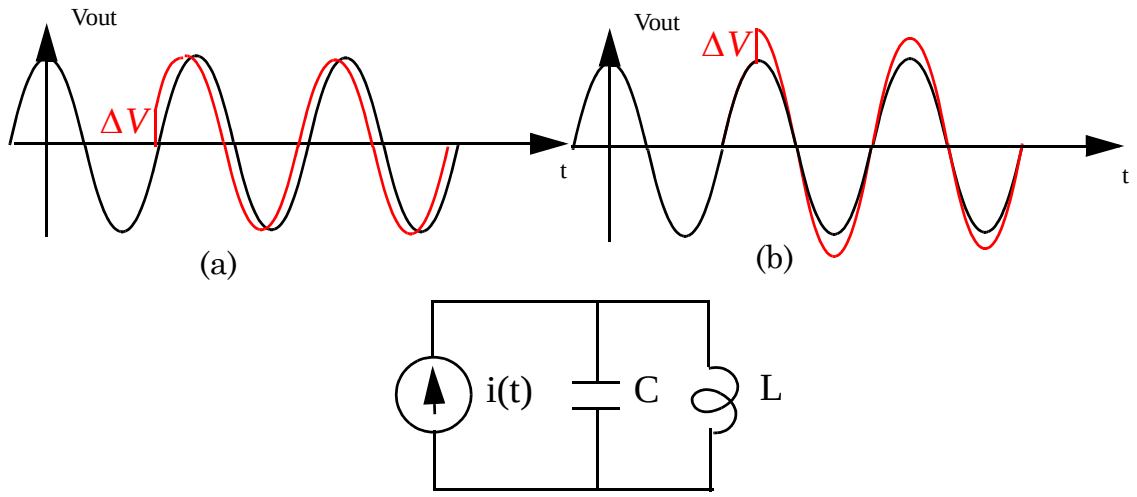

Figure 3-6 Impulse response of ideal LC oscillator for (a) inpulse injected at zero crossings, and (b) impulse injected at wave peak

amplitude current injector *i(t).* Using the superposition integral we arrive at

$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_o}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau)\cos(n\omega_0\tau)d\tau\right]. \quad (3\text{-}5)$$

This expression is very useful in determining the phase noise spectrum resulting from known noise sources. The consequences of this expression can be visualized more easily with the illustration in Figure 3-7. Graph (a) shows a typical plot for the noise spectral density of a MOS transistor. It shows a flat region which is caused by thermal noise, and a *1/f* region that is the result of device flicker noise[2]. Graph (b) shows how the phase noise close to the carrier is a result of the folding of device noise centered at integer multiples of the carrier frequency. This frequency conversion is weighted by $\{c_1, c_2, ..., c_{oo}\}$, the Fourier coefficients of the ISF. Moreover, the upconversion of device *1/f* noise occurs through $\Gamma_{dc} = c_0/2$, the DC value of the ISF[3]. However, Γ_{dc} is governed by the symmetry properties of the single-ended output waveform. The Hajimiri

2. For the purposes of this example, all other noise sources are neglected.
3. Any low-frequency noise sources such as those coupled through the substrate or power supply are also upconverted into oscillator phase noise via Γ_{dc}.

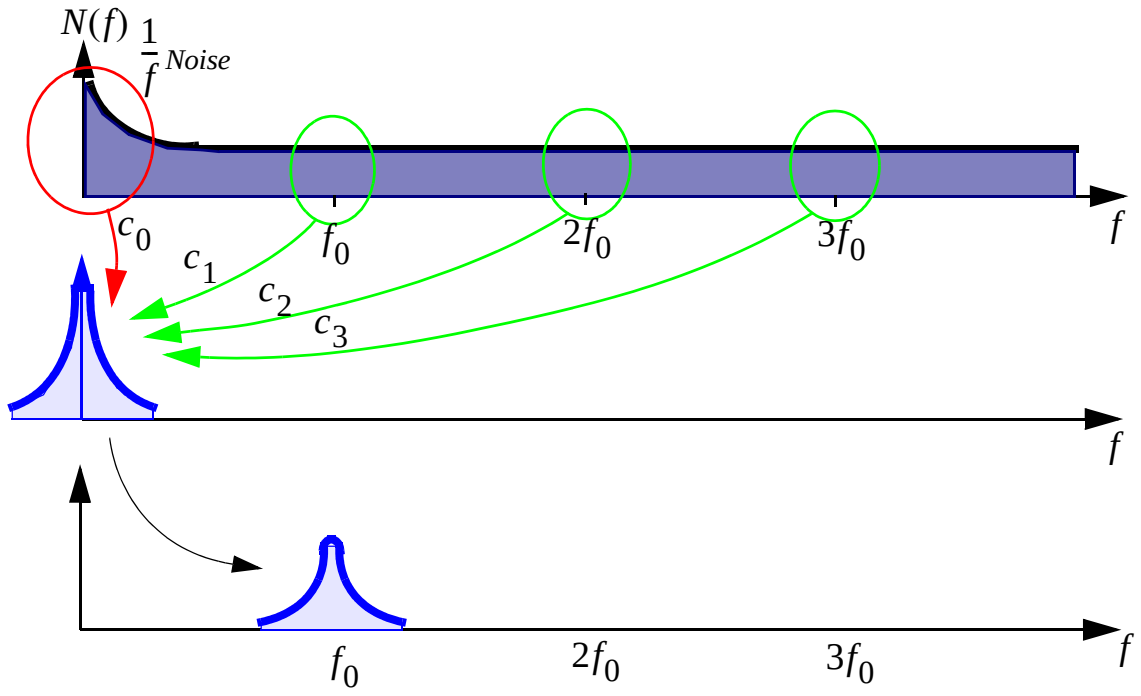

Figure 3-7 Conversion of device noise into oscillator phase noise: (a) MOS device noise spectra; (b) Conversion of device noise to excess phase fluctuations; (c) Carrier modulated by phase noise

model thus predicts the upconversion of *1/f* device noise into close-in phase noise as a function of the symmetry of the output waveform

Finally, Figure 3-8 summarizes the predicted oscillator's single sideband phase noise spectral density. Phase noise in the $1/f^2$ region is due to upconverted thermal noise around the frequency of the carrier and its harmonics and is given by

$$\mathcal{L}(\Delta f) = 10 \cdot \log\left\{\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{i_n^2/\Delta f}{2 \cdot (2\pi\Delta f)^2}\right\} \text{ dBc/Hz,} \qquad (3\text{-}6)$$

where Γ_{rms} is the RMS value of the ISF. Futhermore, phase noise in the $1/f^3$ region is due to device *1/f* noise upconverted by the DC component of the ISF. It is commonly assumed that the $1/f^3$ corner frequency is the same as the *1/f* corner of the device noise spectrum. This is not always the case, as the $1/f^3$

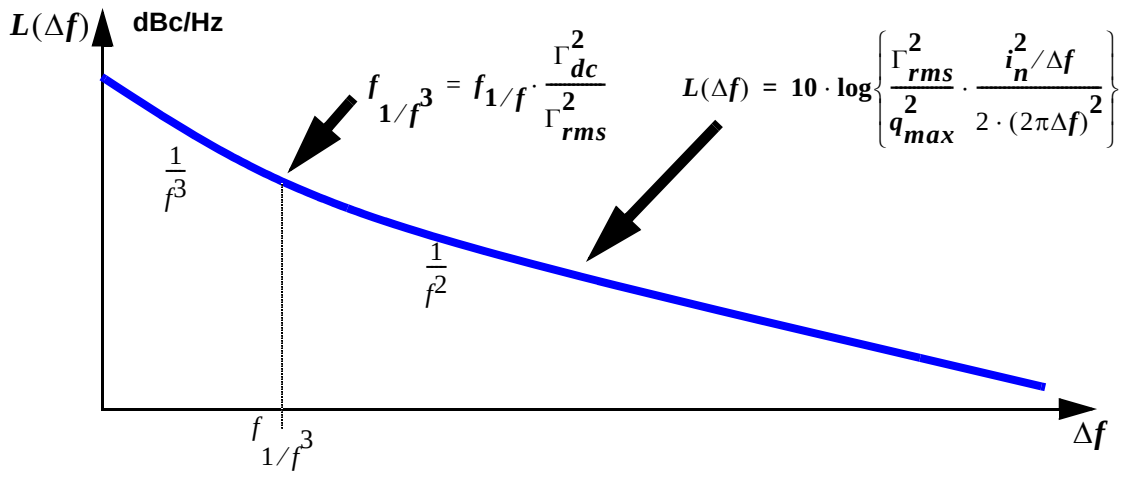

Figure 3-8 Single-sideband phase noise spectrum predicted by Hajimiri's model

corner is actually given by:

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \tag{3-7}$$

where Γ_{dc} is the DC value of the ISF. Only when the DC and RMS values of the ISF coincide will the $1/f^3$ corner be the same as the $1/f$ corner of the device noise spectrum.

Now we are interested in deriving an expression for the single-sideband phase noise of differential ring oscillators. First, we need to determine the ISF and then calculate both the DC and RMS values of the ISF. With this information we can then use equations 3-6 and 3-7 to determine the phase noise and $1/f^3$ corner for the ring oscillator. Figure 3-9 shows a typical ring oscillator waveform (a) with its corresponding ISF (b). We can observe a high sensitivity to noise at the transitions of the output waveform. Using Figure 3-9 (c) we can approximate the DC and RMS values for the ISF shown in (b). Using this

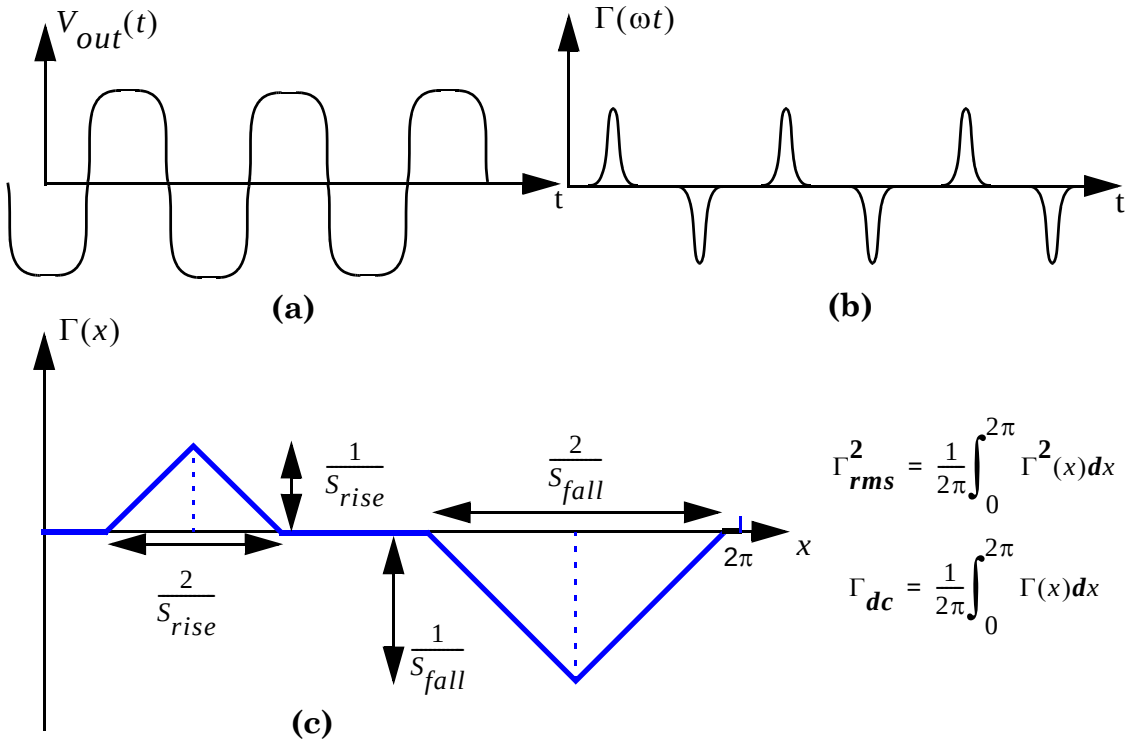

Figure 3-9 Ring oscillator sensitivity to noise: (a) output waveform; (b) Impulse sensitivity function; (c) Graphical approximation of normalized ISF

graph, we derive the DC to RMS ratio for the ISF,

$$\frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} = \frac{3}{2N} \cdot \frac{(1-\beta)^2}{(1-\beta+\beta^2)}, \tag{3-8}$$

where S is the maximum slope of the normalized output waveform, N is the number of stages, and $\beta = S_{rise}/S_{fall}$. This factor is what governs the upconversion of low frequency noise. This analysis shows that for a perfectly symmetric waveform (Γ_{dc}=0) there is no upconversion of flicker noise into phase noise. This result is very interesting in light of the common assumption that oscillators implemented in CMOS will have significant phase noise due to device flicker noise. This is not true if the waveform has good symmetry (in the ISF sense).

Using Equation 3-6, we may derive the following lower bound on the

single-sideband phase noise in the $1/f^2$ region for a differential ring oscillator using short-channel devices:

$$L\{\Delta f\} \geq \frac{18kTV_{dd}}{\pi^2 P} \cdot \left(\frac{2.5}{E_C L_{eff}} + 1\right) \cdot \left(\frac{f_o}{\Delta f}\right)^2 \cdot N \ , \tag{3-9}$$

where P is the power dissipation given by Equation 3-1, E_C is the critical field in silicon, and L_{eff} is the gate length of the differential-pair devices. We can observe that phase noise is a strong function of the number of stages, which justifies the use of 3 to 5 stage ring oscillators. In this study we have selected a 4-stage design. It is important to note that this result applies only to differential ring oscillators. For single-ended CMOS ring oscillators there is no strong dependence of phase noise on the number of stages.

To study the trade-off between phase noise and power dissipation we use equations 3-1 and 3-2 to plot the curve for power dissipation vs. frequency (Figure 3-2) for the topology shown in Figure 3-1, using NMOS differential pair devices of different widths W_n. Figure 3-10 shows the corresponding $1/f^2$ phase noise bound given by Equation 3-9 using a frequency offset from the carrier of 100kHz. We assume a typical 0.5μm CMOS process (Leff=0.5μm) with Vdd=3.3V, critical field, Ec=5.6x10^6V/m, and device flicker noise corner frequency, $f_{1/f}$,of 3MHz. We further assumed all minimum length short-channel devices, PMOS triode load device width twice the width of the NMOS differential pair devices (Wp=2Wn), and oscillator voltage swing given by the replica-bias circuit of Figure 3-1, where V_S= (V_{DD} - V_{CTL}).

In this topology, the swing V_S increases with frequency, which increases the power dissipation, hence lowering the phase noise. Still, the net effect on phase noise is an increase with frequency as predicted by Equation 3-9. In this

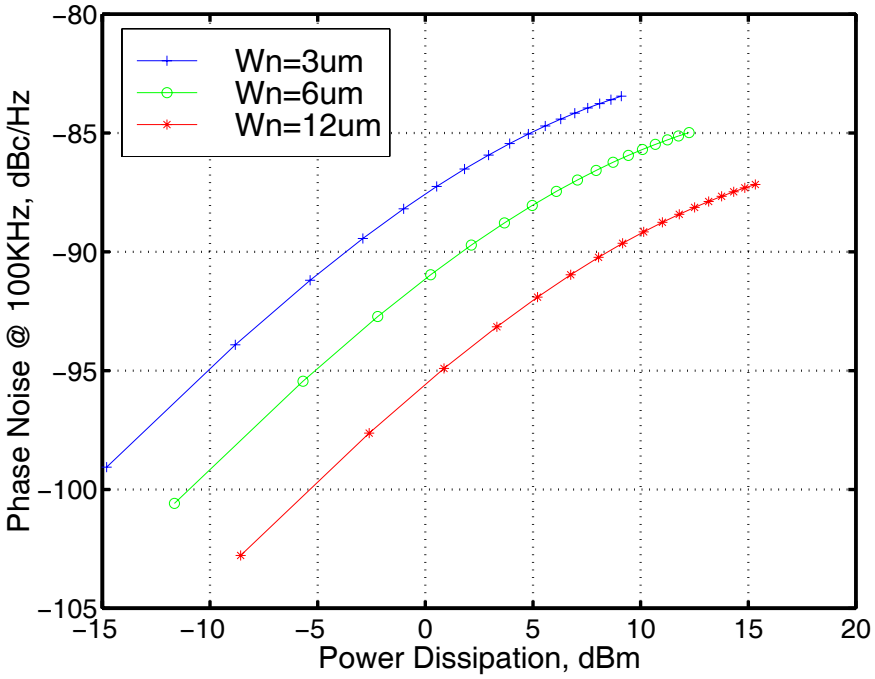

Figure 3-10. Phase noise versus power dissipation of differential ring oscillator

study we select the Wn=6μm curve for an oscillation frequency of 200MHz at a power level of 2.1dBm (1.6mW @ 3.3V) with single-sideband phase noise of -90dBc/Hz at 100kHz offset from the carrier.

3.2.3 Differential Buffer Topology

We next consider three different ring oscillators topologies, each using a different PMOS load circuit for the delay buffer stage: VCO_1-clamped load, VCO_2-symmetric load, and VCO_3-cross-coupled load, respectively (see Figure 3-11). In this section, we examine the impact on phase noise of using these different loads.

The differential buffer (Figure 3-11a) used in VCO_1 has excellent noise and power supply rejection characteristics [Horowitz93]. The cross-coupled diodes (M1, M2) clamp the output swing making the buffer delay insensitive to common-mode noise.

Symmetric load buffers (Figure 3-11b), as used in VCO_2, also have very good supply noise rejection characteristics and have been used extensively in PLL and clock generator designs [Maneatis96]. The graph in Figure 3-11b shows how the load is linearized using a diode-connected transistor (M1) in parallel with a load (M3). The replica bias circuit guarantees symmetry by ensuring that M3 is always in the triode region.

For the proposed cross-coupled load (Figure 3-11c) design of VCO_3, transistor M1 is split into a diode-connected device M1 and a cross-coupled device M2 which increases the overal impedance of the load. This has a side effect of increasing both the gain and the delay through the buffer, thus reducing the oscillation frequency for a given V_C. We start with a symmetric load stage with no cross-coupling and sweep the width of the cross-coupling devices while maintaining the total width (W1+W2=W3=6μm) of the loads constant.

The maximum symmetry of the output waveform is observed when the widths of M1 and M2 are equal to half the width of M3. The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases.

3.2.4 Experimental Results

A more detailed noise analysis is performed to compare the three topologies [Betancourt98a]. The predicted phase noise for a 4-stage oscillator due to thermal noise ($1/f^2$ region) is given by::

$$L\{\Delta f\} = \frac{\Gamma_{rms}^2}{(\pi V_s C_L \Delta f)^2} \cdot \frac{\overline{i_n^2}}{\Delta f}, \qquad (3\text{-}10)$$

where $\overline{i_n^2}/\Delta f$ is the total noise contribution from all sources referred to the

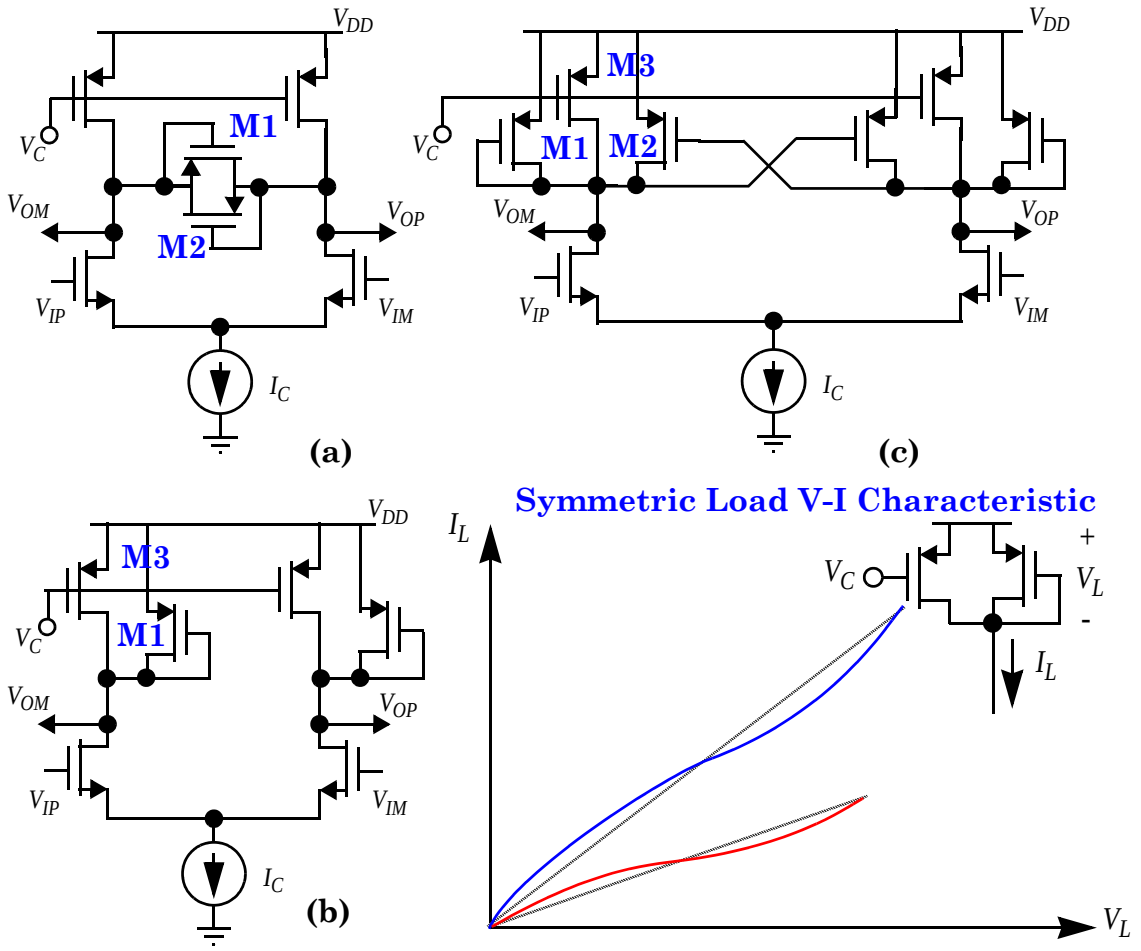

Figure 3-11 Voltage-controlled ring oscillator differential buffer topologies: (a) clamped load, (b) symmetric load, and (c) cross-coupled load

output of the buffer, C_L is the total capacitance at the output node of the buffer, and V_S is the voltage swing across C_L. Figure 3-12 shows the predicted phase noise for VCO1, VCO2, and VCO3. We can observe that the $1/f^2$ regions are within 2.6dB of each other as is to be expected for noise sources of similar size. The model also predicts lower phase noise in the $1/f^3$ region for VCO_3, as it has better symmetry than the other two.

Table 3-1 shows the phase noise at 100kHz offset, and the $1/f^3$ corner frequency for all three oscillators running at 200MHz. Note that, as expected due to the better symmetry, the $1/f^3$ corner for VCO_3 is 95% lower than that of

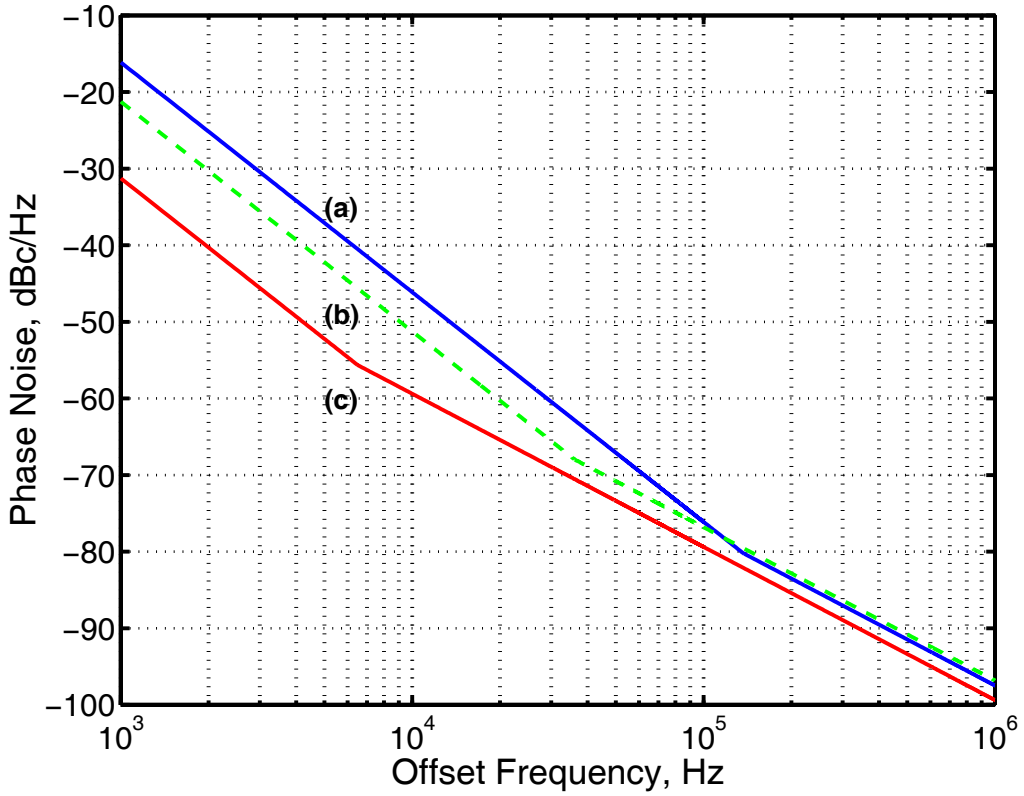

Figure 3-12 Predicted phase noise characteristic for differential voltage-controlled ring oscillators: (a) VCO_1, clamped load; (2) VCO_2, symmetric load; (c) VCO_3, cross-coupled load

VCO_1. These theoretical phase noise and power vs. frequency characteristics are in good agreement with those reported previously [Betancourt97] for VCO_1.

A test chip was fabricated through the MOSIS service using the Hewlett-Packard 0.5μm CMOS process (Figure 3-13). The VCO_1 voltage-to-frequency transfer characteristics measurements for different supply voltages are presented in Figure 3-14. Test results for VCO_1 are shown in Figure 3-15 for

Oscillator	Buffer Topology	$1/f^3$ corner, (kHz)	L{100kHz}, (dBc/Hz)
VCO_1	Clamped Load	137	-75
VCO_2	Symmetric Load	36	-77
VCO_3	Cross-coupled Load	6.5	-80

Table 3-1: Theoretical phase noise and $1/f^3$ corner frequency for VCO_1, VCO_2, VCO_3

operation at 150.9MHz, along with the phase noise predicted by the model. The measured phase noise was -103.9dBc/Hz for a 500KHz offset is very close to the predicted value of -103.2dBc/Hz (Figure 3-15).

These results are well within the 2dB measurement accuracy of the RDL NTS-1000A instrument used. Due to a layout error that caused instability in the replica bias circuit, the phase noise for VCO_2 and VCO_3 could not be measured accurately.

3.3 Summary

To minimize power dissipation of the VCO, a design technique based on a new phase noise model was presented. Furthermore, we compared the phase noise performance of three differential buffer stages. Finally, in this study we proposed a cross-coupled load buffer that achieves lower phase noise in the $1/f^3$ region by exploiting single-ended symmetry in the oscillator's waveform.

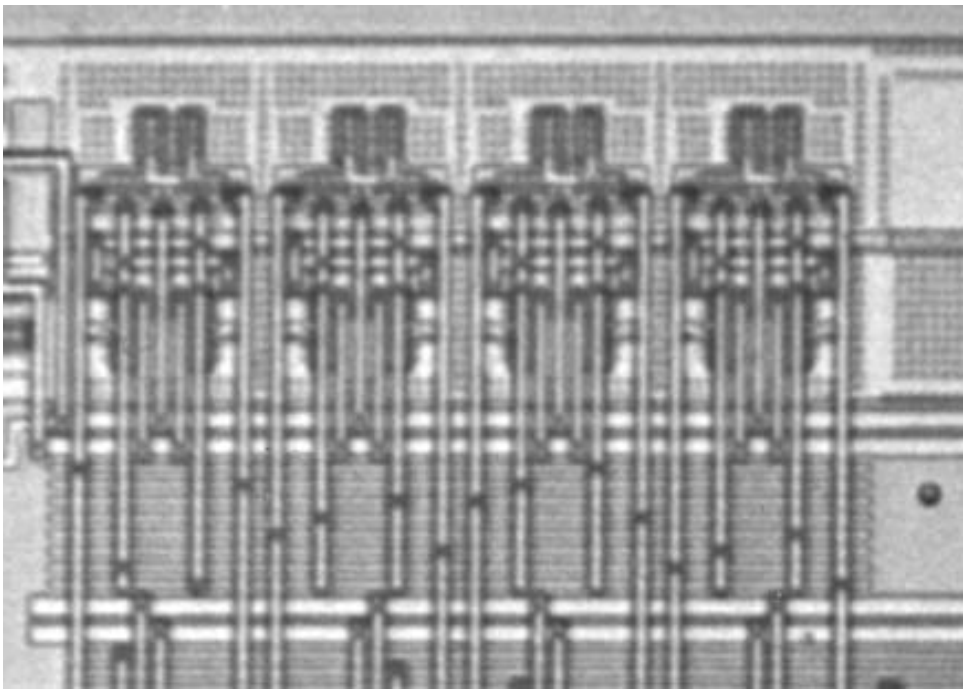

Figure 3-13 Photomicrograph of VCO_3: differential delay buffer cell with cross-coupled loads

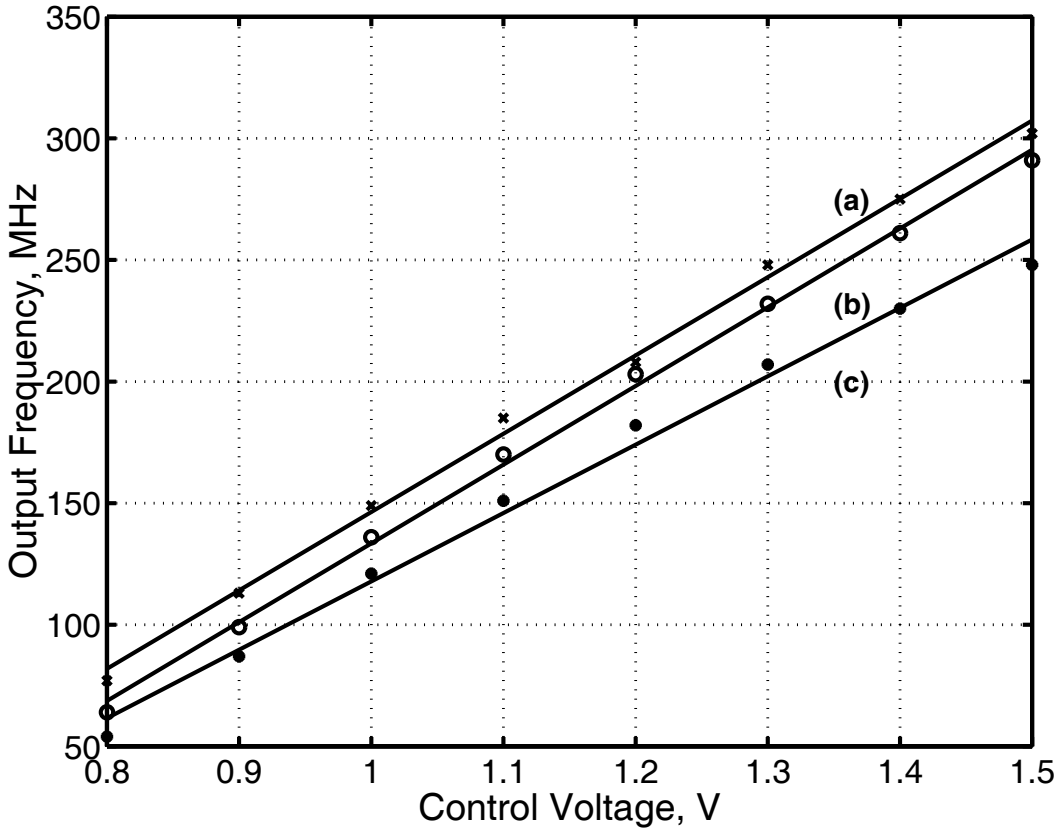

Figure 3-14 Frequency vs. voltage characteristic for VCO_1: (a)VDD=3.0V, (b)VDD=2.7V, (c)VDD=1.8V

3.4 References

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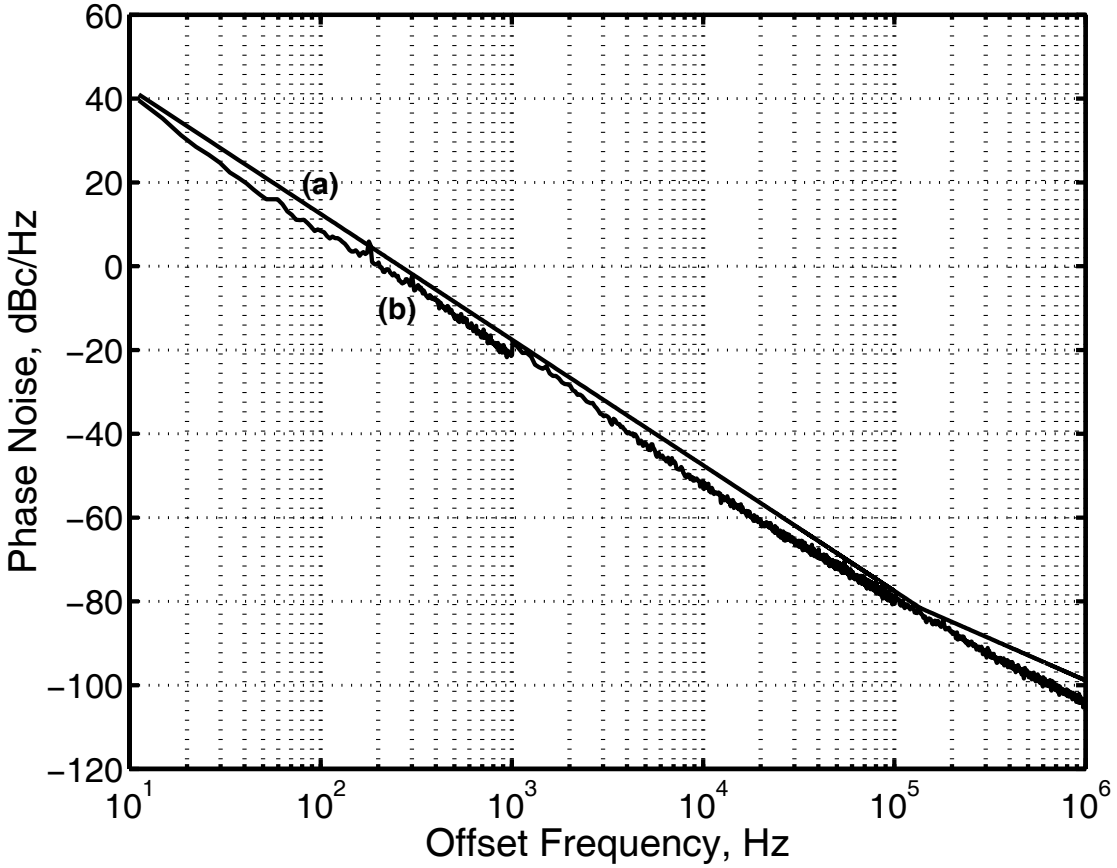

Figure 3-15 Single-sideband phase noise for VCO_1 at 150.9MHz: (a) predicted, (b) measured

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Chapter 4

Injection-locked Frequency Dividers

In this chapter we discuss the theory, modeling, and implementation of frequency dividers that can operate up to 2.8-GHz by exploiting injection locking phenomena in differential CMOS ring oscillators. We show test results for a 5-stage, 1-GHz injection-locked modulo-8 prescaler fabricated in a 0.24-μm CMOS technology that consumes 350 μW of power and occupies 0.012 mm^2 of die area. The input-referred locking range is 20 MHz and the locked phase noise is -110 dBc/Hz @ 100 kHz. A 2.8-GHz, 3-stage, modulo-4 divider is also discussed.

4.1 Background

As we have stated previously, significant portion of the power budget for any RFIC system is allocated to the generation of the RF carrier and local oscillator (LO) in monolithic frequency synthesizers. The major sources of power dissipation in a frequency synthesizer are the VCO and frequency dividers. In Chapter 3 we discussed a design technique that takes into consideration the power versus phase noise trade-off in differential voltage-controller ring

oscillators. There is still a great need for a better understanding of low-power techniques for frequency division which is essential to reduce the overall power dissipation of integrated frequency synthesizers.

In Chapter 2 we discuss the fundamental theory of injection-locked oscillators as described by van der Pol and Adler. This theory also predicts the synchronization of an oscillator to an injected signal which is harmonically related to the free-running oscillation frequency. Thus, using a harmonic locking technique, an injection-locked oscillator can be used as a frequency divider.

Recently, there has been a lot of interest in reducing the power dissipation of integrated frequency dividers, most of which use current mode logic (CML) [Darabi00]. In contrast, integrated injection-locked dividers are commonly used in applications where the frequency of operation is very high, beyond what can be achieved with flip-flop based circuits. Efforts at frequencies beyond 5 GHz have been reported using injection-locking to implement divide-by-2 prescalers in CMOS [Rategh00], and Si-BJT [Derksen88] technologies. This principle has also found common use at millimeter-wave frequencies in GaAs [Maligeorgos00] and SiGe technologies [Kudszus00].

In this chapter, we propose a technique that exploits injection-locked ring oscillators to achieve low-power frequency division. It has the potential of reducing the power dissipation of frequency division by up to an order of magnitude compared to conventional digital solutions. To demonstrate this technique, we use injection-locking in CMOS ring oscillator frequency dividers that can operate at frequencies of up to 2.8 GHz [Betancourt01][1]. We also present a model for injection-locked frequency dividers (ILFDs) that predicts the locking

1. The frequency was limited by the specific circuit implementation not choice of technology.

range and shows design insights that enable further optimization.

4.2 Modeling

The basic idea behind frequency regeneration is to create an oscillation at a subharmonic of the input signal with the aid of a feedback network. This phenomenon has been known for decades, as pointed out in Chapter 2.

In 1939 Miller described a regenerative frequency divider based on this principle [Miller39]. A qualitative understanding can be obtained from the modulo-2 Miller divider shown in Figure 4-1. It is assumed that there is a harmonic component of the injected signal initially present in the feedback path to start the oscillation. The origin of such a signal can be thermal noise or the transient that takes place when the input is initially injected into the circuit. By feeding back ω_{OUT} into a mixer with input ω_{RF}, sidebands at ω_{OUT} and $3\omega_{OUT}$ are created (since $\omega_{OUT} = \frac{1}{2}\ \omega_{RF}$). Filtering out $3\omega_{OUT}$, the output at $\frac{1}{2}\ \omega_{RF}$ builds up and the oscillation is sustained.

Miller's divider can achieve division ratios greater than two by including a harmonic generator or frequency multiplier in the feedback path. This frequency multiplier does not have to be explicit, as it can be provided by non-linearities already present in the circuit. As shown in Figure 4-2, an (M-1) frequency multiplier can be used to generate an output frequency of ω_{RF}/M.

For the Miller divider to work, the open-loop gain must exceed unity to sustain oscillation at the desired output frequency when the input signal is present, and the gain must be smaller than one in the absence of the input to ensure no spurious oscillations. In other words, the Barkhausen criteria for oscillation are only met in the presence of an injected signal. This is in contrast

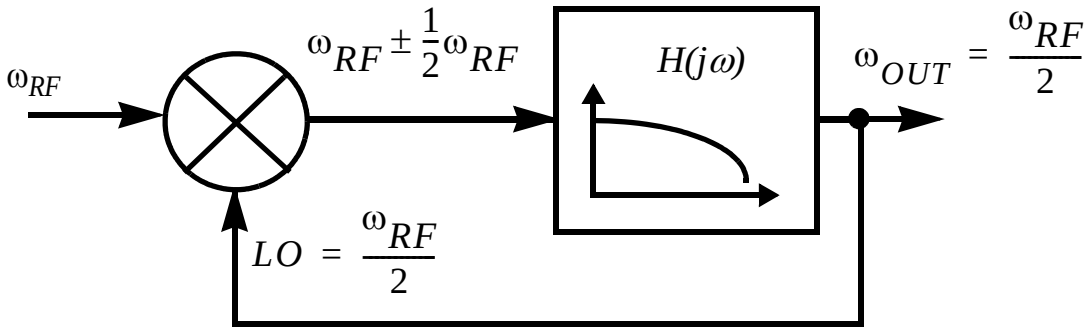

Figure 4-1 Model for modulo-2 Miller regenerative frequency divider

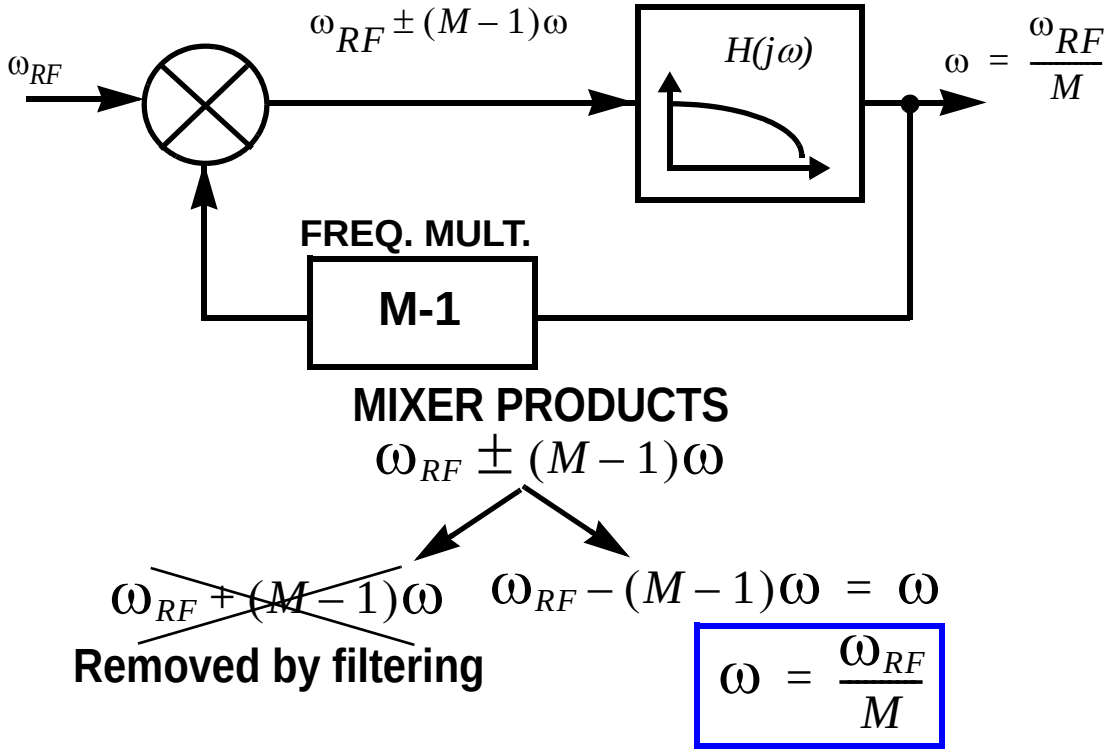

Figure 4-2 Model for modulo-M Miller regenerative frequency divider

to a divider based on a harmonically-locked oscillator, which always produces an output even in the absence of an injected signal. Nevertheless, we can describe both the Miller and harmonic-locked dividers using a generalized mixer-based model similar to Miller's, since the locking mechanisms and equations that describe their behavior are identical. Moreover, both the Miller and the injection-locked dividers are special cases of a harmonically-locked feedback

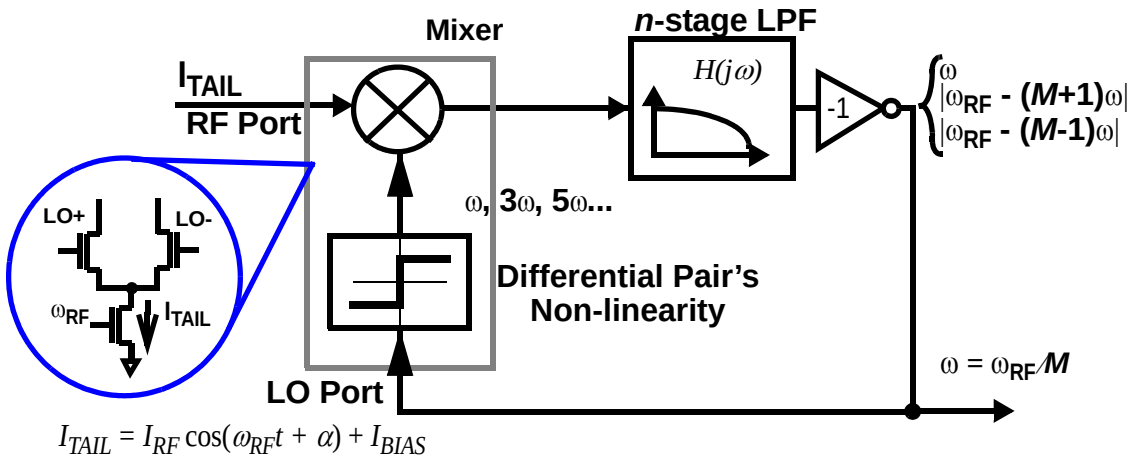

Figure 4-3 Generalized model of injection-locked frequency divider

system.

A simplified block diagram representing a harmonically-locked feedback system is presented in Figure 4-3. Modeling of this system is complicated by the presence of a nonlinear element, the mixer[2]. Nonlinear functions can be approximated by a quasi-linearization technique using describing functions. Describing function theory and techniques represent a powerful mathematical approach for analyzing the behavior of nonlinear systems [Taylor99]. In this approach, a deterministic, single frequency sinusoidal input excites the nonlinearity and the output is described by the first term of a Fourier series (harmonic linearization). This kind of description is comparable to the frequency response function in linear systems, but the gain is not constant and depends on the amplitude of the input signal.

For this model, we assume a single-balanced mixer based on a differential-pair. The input voltage signal of frequency ω_{RF} is injected into the tail device ("Injector") of the differential pair, which produces an RF current which

2. To be precise, not all mixers are nonlinear—most are actually linear, but time-varying.

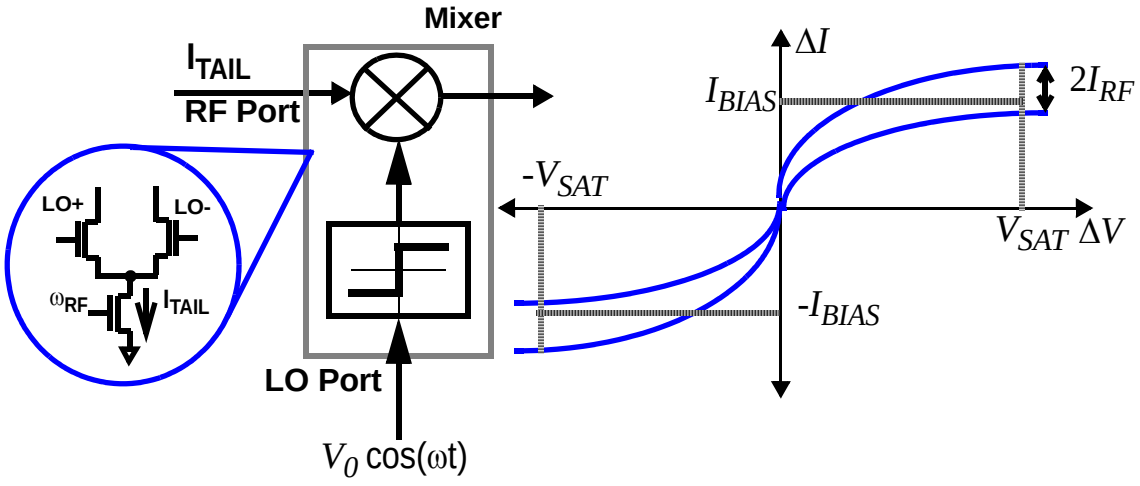

Figure 4-4 Transfer characteristic of the differential pair mixer

adds to the I_{BIAS} current flowing into the differential pair ("Mixer"). In general, due to non-linearity of the Injector, this RF current will include a DC component and all harmonics of ω_{RF}. For now, we assume linear operation of the Injector, and ignore the DC component and higher harmonics of ω_{RF}. For $\omega_0 = \omega_{RF}/M$, the input-referred phase (α) is defined over the single-sided interval $(-\pi,\pi]$.

Assuming perfect device matching, the differential-pair's transfer characteristic is non-linear with odd symmetry, as shown in Figure 4-4. When excited by the ILFD's output at ω_0, the mixer's non-linearity produce odd harmonics at $3\omega_0$, $5\omega_0$, etc. Therefore, the total current in the tail due to the bias and injected signals (I_{TAIL}) is modulated by ω_0 and its harmonics. The mixer products are filtered and amplified by $H(j\omega)$, which models the low-pass filtering action of n amplifier stages. In the case of a ring oscillator, this low-pass behavior is due to the interaction of the output impedance of each buffer with the input capacitance of the following stage. We assume that the filter substantially suppresses the output products of the mixer whose frequency is higher than ω_0.

Hence, the output voltage V_O is sinusoidal. This is a fairly good approximation as long as the number of stages is small. This output at ω_0 is fed back to the mixer's LO port, and closes the loop. Note that there is also one net inversion around the loop.

4.2.1 Locking Range

One of the limitations of ILFD's is their limited frequency operating range. The locking range defines how far the injected signal can deviate from the free-running frequency of the oscillator while maintaining synchronization with the injected signal. To quantify the locking range of the Miller divider, first we determine the open-loop transfer characteristic and separate it into phase and magnitude components.

The ILFD maintains lock as long as there is an injected signal at ω_{RF} with sufficient strength. While injection-locked, the output ω_0 tracks ω_{RF}/M within the locking range of the divider. When there is no signal injection, the ILFD free-runs and ω_0 is solely determined by circuit parameters. If there is sufficient gain around the loop, the output amplitude V_O is always large— even at the edge of the ILFD's locking range. In this case, the injection locking dynamics are determined primarily by the phase relationship around the loop (the range is phase-limited) and therefore we can ignore the amplitude expression. A large amplitude is also required to excite the mixer's LO port non-linearity, which is the mechanism that makes possible division ratios greater than two.

Keeping these issues in mind, we now describe in detail the modeling of each component and derive an expression for the locking range of the ring oscillator frequency divider. As derived in Chapter 2, Equation (2-12), the

low-pass open loop transfer function of the ring oscillator, $H(j\omega)$, can be modeled by:

$$H(j\omega) = \frac{H_o}{\left(1 + \frac{j\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right)^n}, \tag{4-1}$$

where ω_0 is the natural frequency of the free-running oscillator. Each stage contributes π/n to the phase, resulting in a total phase lag of 2π around the loop (including the inversion). The filter gain constant H_0 does not affect the subsequent phase calculations.

The differential pair in the single-balanced mixer has the transfer characteristic shown in Figure 4-4. For square-law devices, the differential pair's saturation voltage V_{SAT} is defined by:

$$V_{SAT} = \sqrt{\frac{(W/L)_{DIFF}}{(W/L)_{TAIL}}} \cdot V_{OD}, \tag{4-2}$$

where $(W/L)_{DIFF}$ and $(W/L)_{TAIL}$ refer to the sizes of the differential pair and tail devices, respectively, and V_{OD} is the overdrive voltage (V_{GS}-V_T) of the tail device. If the voltage swing V_O is large compared to V_{SAT}, the differential pair switches abruptly and in the asymptotic limit, the output of the mixer becomes

$$\Pi(t) \cdot [I_{RF} \cdot \cos(\omega t + \alpha) + I_{BIAS}], \tag{4-3}$$

where the mixing function $\Pi(t)$ is a square-wave. Therefore, the Fourier coefficients C_k of the mixing function can be approximated by:

$$C_k = \begin{cases} \frac{1}{k\pi} \cdot (-1)^{(k-1)/2} & \text{for } k = \text{odd} \\ 0 & \text{otherwise} \end{cases} \tag{4-4}$$

Writing the phase expression around the loop in Fig. 1, we get

$$\operatorname{atan}\left(\frac{\eta_i(C_{M-1}-C_{M+1})\sin\alpha}{C_1+\eta_i(C_{M-1}+C_{M+1})\cos\alpha}\right)=\angle H(j\omega)-\pi = n\operatorname{atan}\left(\frac{\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right)-\pi \quad (4\text{-}5)$$

$$\eta_i = \frac{I_{RF}}{2I_{BIAS}}, \quad (4\text{-}6)$$

where M is the division ratio, and η_i is the injection efficiency. Using the C_k coefficients from (4-4), (4-5) can be solved exactly for the set of values ω/ω_0 which yield a solution for α in the range (-π,π]. To get an approximate analytical expression, we linearize the phase response of the filter around ω_0 as shown in Chapter 2, Equations (2-24) through (2-26):

$$\phi \cong \pi + S\cdot\Delta\omega = \pi + \frac{n\sin\left(\frac{2\pi}{n}\right)}{2}\cdot\frac{\Delta\omega}{\omega_0}, \quad (4\text{-}7)$$

where ϕ is the phase around the loop, and $\Delta\omega = \omega - \omega_0$. The phase-limited locking range is given by the maximum difference $\Delta\omega/\omega_0$ that satisfies the conditions of (4-5). Using (4-7), we can write the following analytical expression for the locking range, $\Delta\omega/\omega_0$:

$$\frac{\Delta\omega}{\omega_0}\cong\frac{4}{n\sin\left(\frac{2\pi}{n}\right)}\operatorname{atan}\left(\frac{k_0}{\sqrt{1-k_1^{\,2}}}\right), \quad (4\text{-}8)$$

$$\text{where } k_0 = \eta_i\left|\frac{C_{M-1}-C_{M+1}}{C_1}\right| \quad (4\text{-}9)$$

$$\text{and } k_1 = \eta_i\left|\frac{C_{M-1}+C_{M+1}}{C_1}\right|. \quad (4\text{-}10)$$

In expression (4-8) we can clearly see the fundamental trade-offs associated with an ILFD. The locking range is a function of injection efficiency η_i and the magnitude of the Fourier coefficients C_{M-1} and C_{M+1}. Note that $k_1^{\,2}$ is usually much smaller than one. From (4-4) it is obvious that C_{M-1} and C_{M+1}, which

are of opposite signs, will tend to cancel each other when summed together. For a small injected signal ($\eta_i \ll 1$), the locking range increases linearly with the injected signal strength. Typical injection efficiency η_i of an ILFD is around 0.5.

We also observe from (4-7) that $n\sin(2\pi/n)$ is proportional to the slope of the phase $d\phi/d\omega$ of the filter $H(j\omega)$. Thus, the locking range is inversely proportional to this slope and hence to the number of stages n.

Our initial assumption is that the mixer's switching function is a square wave. This is accurate if the swing ratio $\rho_s = V_0/V_{SAT}$ is much larger than 1. However, if that assumption does not hold well, the magnitudes of the Fourier coefficients canreduce significantly. For intance, as ρ_s gets smaller, the square wave assumption is no longer valid and the coefficient ratios C_k/C_1 are significantly smaller, thus degrading the achievable locking range. Figure 4-5 shows the effect of the swing ratio on the Fourier coefficient ratios, C_k/C_1. Simply put, to increase the locking range we should reduce the number of stages, increase the injected signal's current I_{RF}, and maximize the coefficient ratios C_k/C_1.

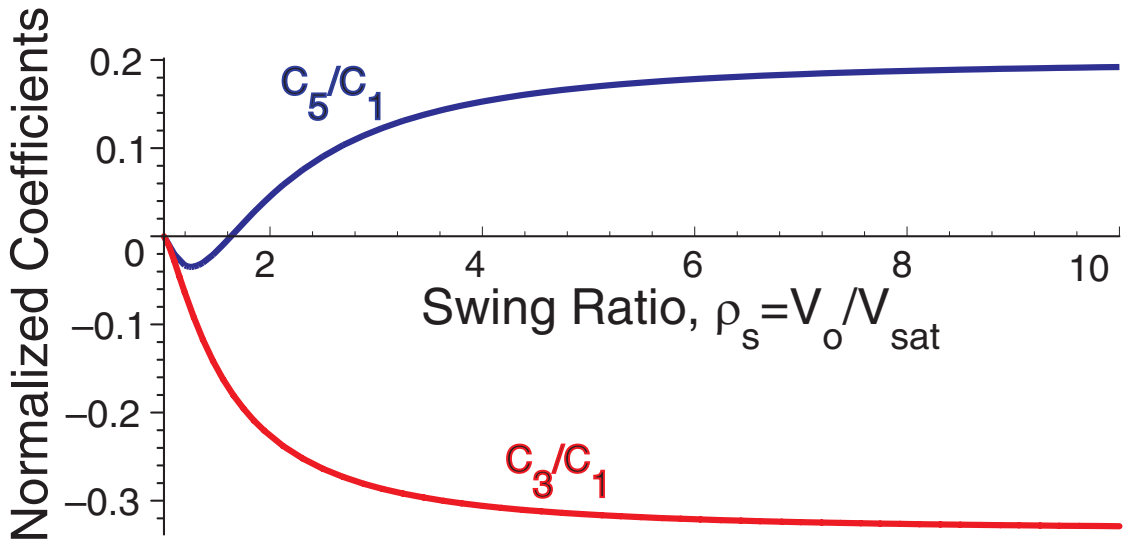

Figure 4-5 The effect of swing ratio ρ_s on Fourier coefficient ratios C_k/C_1.

Now, let's examine other effects that influence the achievable locking range (Figure 4-6). The Injector's efficiency may also be limited by transconductance drop due to velocity saturation, device non-linearity, and drain junction parasitics. Short-channel effects in the Injector cause the device's I-V characteristic to deviate from a square law. Assuming that the active-region characteristic of the tail device is given by $I_{DS} = K \cdot (V_{RF} + V_{OD})^{\gamma}$, we can redefine injection efficiency as:

$$\eta_i = \frac{I_{RF}}{2I_{DC}} = \frac{V_{RF}}{2V_{OD}} \cdot \gamma \tag{4-11}$$

$$\text{and } I_{DC} \cong I_{BIAS}, \tag{4-12}$$

where γ is between 1 and 2. We already know that the locking range is proportional to η_i, and hence to V_{RF}/V_{OD}.

Ideally, the Injector acts like a perfectly linear transconductor, but due to Injector non-linearities, I_{DC} rises for large injected signals ($I_{DC} > I_{BIAS}$), reducing the injection efficiency and leading to compression of the locking range. This may occur for large injected amplitudes, where the Injector is forced into the triode region for part of the cycle. An increase of I_{DC} also affects V_{SAT}, reducing the swing ratio. Both of these effects degrade the locking range.

Finally, parasitic capacitances within the mixer reduce the magnitude of the RF current which feeds into the switching differential pair. Specifically, the capacitance on the drain of the tail device (due to its drain junction and source junctions of the differential pair) provides a shunt path for I_{RF}, reducing η_i at high frequencies. At larger injection amplitudes, the higher current harmonics generated by the Injector would also tend to improve the locking range of the divider over the case where only the fundamental component were

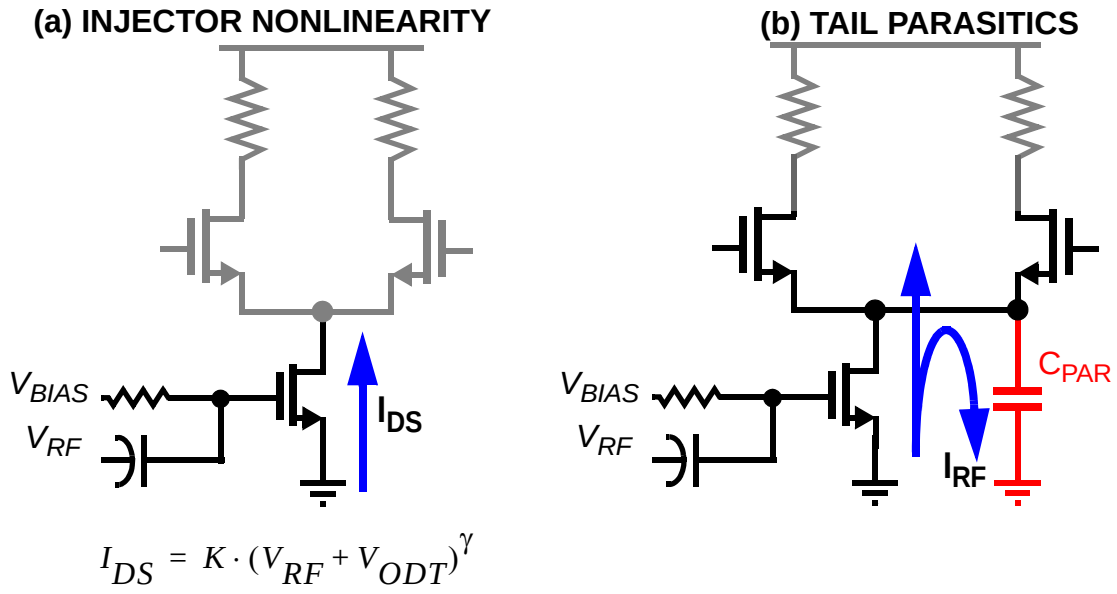

Figure 4-6 Effects of limited injection efficiency and parasitics on locking range: (a) injector nonlinearity; (b) tail transistor parasitic drain capacitance.

present. However, due to parasitics, these harmonics are also suppressed, even more strongly than the fundamental RF component.

Figure 4-7 shows the locking range for a 5-stage, modulo-8 ILFD as a function of the normalized injected signal (V_{RF}/V_{OD}) for the ideal case (a), and when we account for injection efficiency degradation due to Injector non-linearity (b), and for tail drain parasitic capacitance that shunts 50% of the RF current to ground (c).

4.2.2 Transient Response

Aside from the locking range, it is also important to understand the transient response of ILFDs as it reveals much about their phase noise filtering properties. It was Adler who first described the transient response of the oscillator phase as an exponential for weak injection[3]. If the output frequency is

3. See Chapter 2, Equations (2-29), (2-30), and (2-31).

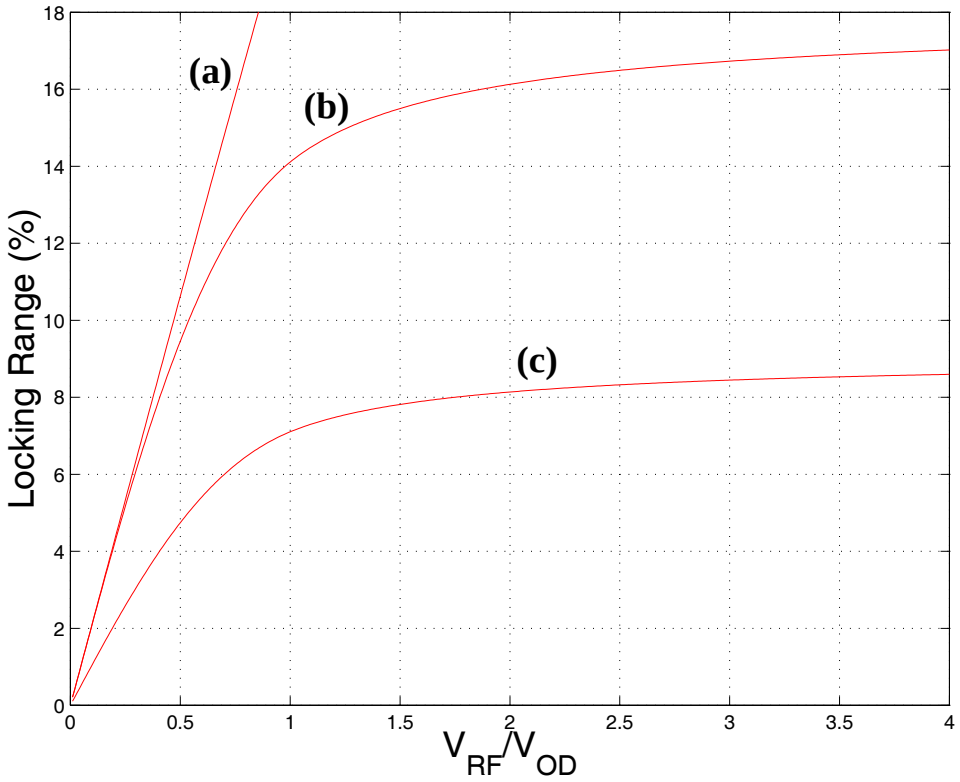

Figure 4-7 Locking range of 5-stage, modulo-8 ILFD: (a) Ideal (phase-limited) case, (b) Compression due to injector nonlinearity, (c) Injector nonlinearity & drain junction parasitics (50% RF current loss).

close to ω_0, and for a small frequency or phase step, a modulo-M ILFD has a first-order transient response with the following time constant [Verma03]:

$$\tau \cong \frac{1}{M}\left|\frac{S}{k_1 - k_0}\right| = \left|\frac{1}{M\Delta\omega}\right|, \tag{4-13}$$

$$\text{where } |\Delta\omega| \cong \frac{1}{\tau M}, \tag{4-14}$$

and the constant S is the linearized slope of the phase transfer function of the filter $H(j\omega)$. We observe from (4-15) that the same parameters affect both the phase-limited locking range and the time constant τ. From (4-16) we conclude that the phase-limited locking range of an ILFD is approximately $1/M$ times the 3-dB bandwidth of the first-order system response. Therefore, maximizing the locking range also results in the fastest transient response [Verma03].

4.2.3 Phase Noise

In an ideal modulo-M divider, the phase noise power spectral density at the output is the same as that of the input signal, divided by M^2. Realistically, any practical divider will add its own noise contribution due to intrinsic device noise as well as power supply noise coupling. We now present without proof the phase noise spectrum of the ILFD as shown by [Verma03].

According to the Hajimiri phase-noise model [Haji98a], the current-to-phase impulse response is given by equation (3-3) (repeated here for convenience):

$$\boldsymbol{h}_{\phi}(\boldsymbol{t},\tau) = \frac{\Gamma(\omega_{\mathbf{0}}\tau)}{\boldsymbol{q_{max}}}\boldsymbol{u}(\boldsymbol{t}-\tau). \tag{4-15}$$

In a free-running oscillator, the phase cannot recover if perturbed, but for injection-locked systems, phase will always recover due to the synchonization mechanism that forces a fixed phase relationship between the injected signal and the output of the ILFD.

For weak injection, the phase impulse response of the ILFD is:

$$\boldsymbol{h}_{\phi}(\boldsymbol{t},\tau) = \frac{\Gamma(\omega_{\mathbf{0}}\tau)}{\boldsymbol{q_{max}}}e^{-t/\tau}, \tag{4-16}$$

where $e^{-t/\tau}$ represents the decaying exponential response of the ILFD with time constat τ given by (4-15). The power spectral density (PSD) of the locked ILFD due to internal noise of the divider in the locked state is given by:

$$L\{\Delta\omega\} = L_{free}\{\Delta\omega\}\cdot\frac{\Delta\omega^2}{\Delta\omega^2+\omega_p^2} + L_{inj}\{\Delta\omega\}\cdot\frac{(\omega_p/M)^2}{\Delta\omega^2+\omega_p^2} \tag{4-17}$$

where $\omega_p = 1/\tau$. The first term is a high-pass filtered version of the intrinsic free-running oscillator phase noise and the second term corresponds to the low-pass filtered phase noise contribution of the injected signal.

We can observe that this noise filtering behavior is similar to that of a PLL (as discussed in Chapter 3), where ω_p is analogous to the PLL's loop-bandwidth. Like the PLL, the ILFD tracks the phase noise of the injected source within its locking range. At frequency offsets far from $\Delta\omega$ the phase noise of the injection-locked oscillator approaches its free-running phase noise. One important difference is that this loop bandwidth is influenced by the strength of the injected signal [Rategh99]. Therefore, we can get large loop bandwidth and fast locking time for strong injection, and low bandwidth with good source phase noise suppression for weak injection.

4.3 Circuit Implementation

To test the theory described in Section 4.2, we design and characterize different ring oscillator injection-locked frequency dividers that use differential buffer delay stages with replica-feedback biasing [Maneatis96]. As described in Chapter 2, tuning of the center frequency is achieved by changing the delay through each cell through biasing. The layout of the ring oscillator is symmetrical and load balanced to minimize any skew between the phases. The two ring oscillators designed have 3 and 5 buffer stages, respectively. Modified cross-coupled symmetric load buffers [Figure 4-8(b)] are used for their good supply noise rejection and low *1/f* noise upconversion characteristics [Betancourt98b].

We inject the RF signal at the gate of the tail current source of the first buffer (Injector), using it as a single-balanced mixer. The mixing action occurs in the differential pair, and the remaining buffer stages behave as a multipole filter $H(j\omega)$ that contributes the gain and phase shift required to sustain the oscillation.

Now, let's discuss the advantages and trade-offs of this implementation.

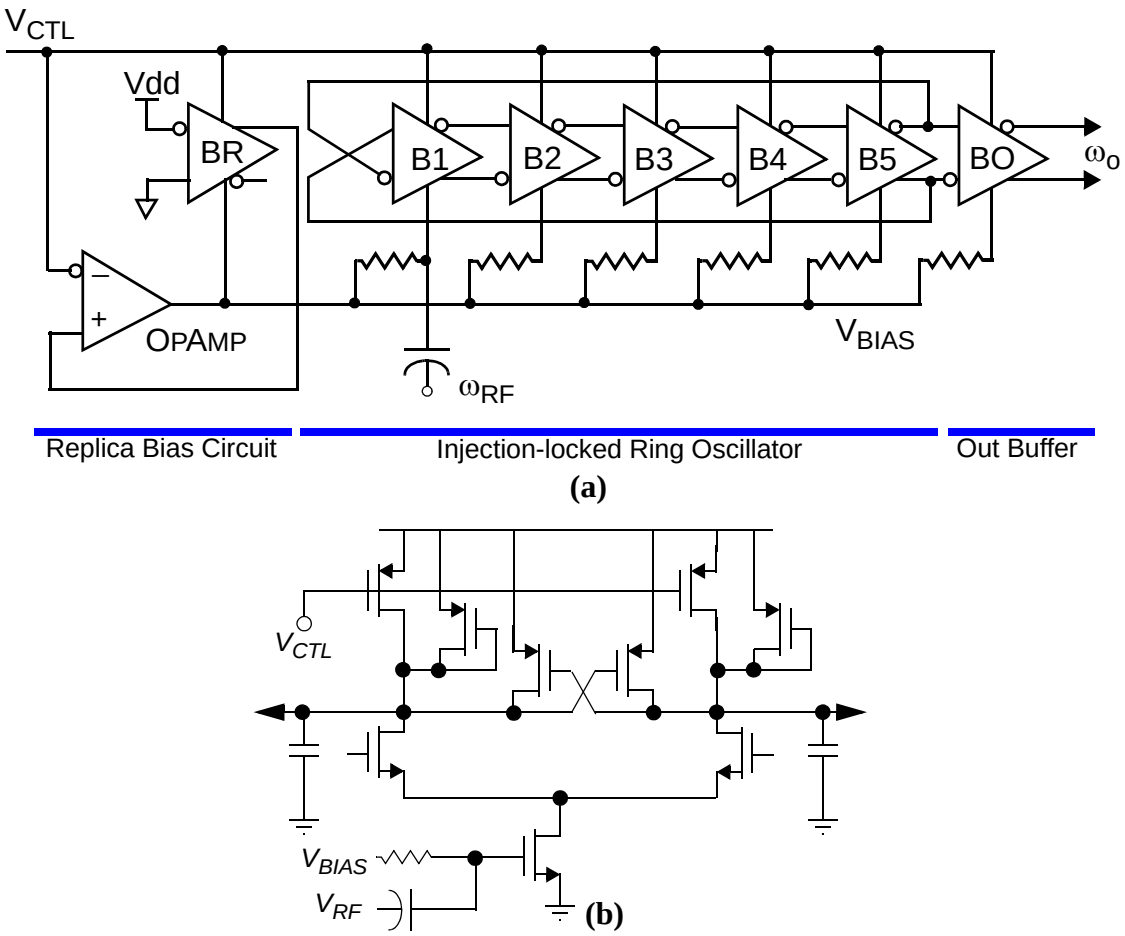

Figure 4-8 Schematic diagram of the ring oscillator injection-locked frequency divider: (a) 5-stage ring oscillator with injection, (b) differential delay buffer using modified cross-coupled symmetric loads.

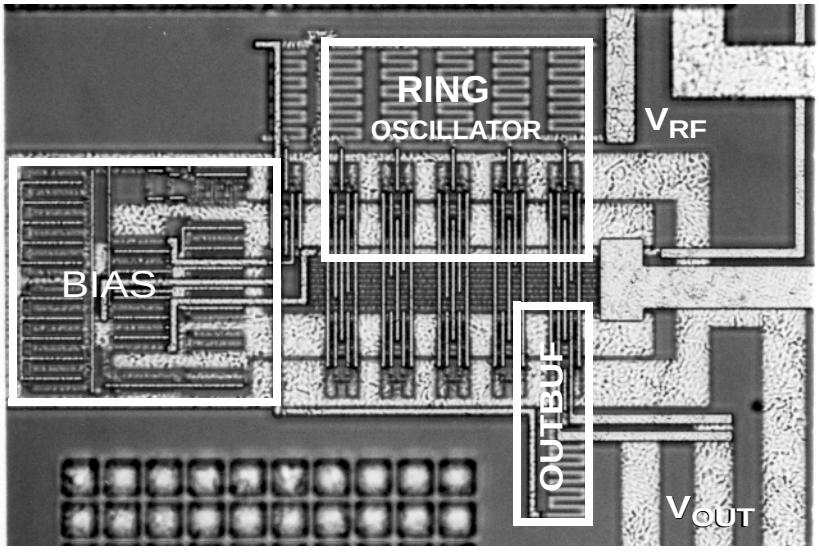

Figure 4-9 Die micrograph of the 5-stage ring oscillator injection-locked frequency divider.

First, ring oscillators are compact, require no external components, and can operate a very low power levels at sub-GHz frequencies. Moreover, every buffer in the ring oscillator ILFD is operating at ω_0, which lowers power dissipation.

Second, while a flip-flop based divider uses more power as we add more stages, the ring oscillator ILFD does not require more stages and furthermore uses less power for higher division ratios. In fact, as we have shown earlier with equation (4-8), a smaller number of stages increases the locking range, making practical division ratios greater than two. Please note that increases in power efficiency come at the expense of a reduction in locking range.

Finally, at multi-GHz frequencies, LC-based injection-locked dividers become feasible, possesing less noise and using less power than ring oscillators [Rategh00], so why not use them in this application? In theory, a single-stage LC oscillator is capable of even lower power operation, but the large area required to integrate the inductors often makes this choice impractical for sub-GHz operation. Resorting to off-chip inductors would compromise our goal of complete integration.

4.4 Experimental Verification

Measured performance of the ring oscillator ILFD is summarized in Table 4-1. A 5-stage, modulo-8 prescaler has been implemented in a 0.24-μm CMOS technology, as shown in the micrograph of Figure 4-9. It occupies 0.012 mm^2 of die area and consumes 233μW of power from a 1.5-V supply. The measured input-referred locking range is 20 MHz at 1 GHz for an injected power of 0 dBm. The 3-stage ILFD achieves an input-referred locking range of 125 MHz at 2.8 GHz (modulo-4) with -5 dBm of injection. It also occupies 0.012 mm^2 of

	5-stage ILFD	***3-stage ILFD***
Injected Frequency	1.0 GHz	2.8 GHz
Free-running Frequency	125 MHz	700 MHz
Phase Noise@100KHz	-110 dBc/Hz	-106 dBc/Hz
Locking Range	***(input referred)***	
Modulo-2	12.7MHz (-3dBm)	125 MHz (-3dBm)
Modulo-4	32 MHz (-3dBm)	56 MHz (-5dBm)
Modulo-6	17 MHz (-3dBm)	no-lock
Modulo-8	20 MHz (-3dBm)	no-lock
Power dissipation		
Vdd	1.5V	3.0V
Icore	233μA	331μA
Ibias	108μA	661μA
Core power	350μW	993μW
Power efficiency	2.86 GHz/mW	2.82 GHz/mW
Implementation		
Die area	$0.012mm^2$	$0.012mm^2$
Technology	0.24-μm CMOS	0.24-μm CMOS
Package	44-pin TQFP	44-pin TQFP

Table 4-1: Measured results of 3-stage and 5-stage ring oscillator injection-locked frequency dividers.

die area and consumes 993μW of power.

As we increase the injected voltage, we eventually drive the tail device into its cut-off region for part of the cycle. Hence, we excite the nonlinearity of the injection transistor, and the RF energy gets "spread" into other harmonics and the DC component, effectively lowering the injection efficiency η_i. This can be observed as saturation of the locking range, predicted by the model and confirmed in simulations (Figure 4-7). The eventual compression of the locking range also occurs due to the large amplitude of the signal being injected. In this case, the Injector is forced into the triode region for part of the cycle, reducing the effective transconductance. Given the large Injector size (W/L =10μm/1μm) and small V_{OD} of our implementation (10 mV), short-channel effects are

probably negligible.

Parasitics in the tail node reduce significantly the locking range as they steal some of the injected signal power. Parasitic capacitance at the tail transistor drain junction is significant in our implementation and can be reduced by scaling the tail transistor more aggressively, and/or resonating the tail node capacitance [Wu01].

Because the achieved swing is smaller than expected, the locking range measured differs substantially from what is predicted by our model. The smaller swing breaks the assumption that the mixer function is a square wave, hence the magnitudes of the Fourier coefficients get reduced significantly. For smaller than expected oscillation amplitude this implies a reduction in the locking range, as was shown in the measurements. Simply put, simulation models proved to be too optimistic, hence the locking range is smaller than predicted by Spice (Table 4-2).

Finally, we also observe that the locking range is not always symmetric around the free-running frequency, especially at higher injected power levels. This behavior is due to the increase of I_{DC} with the injected signal. Our ring oscillator buffers are current controlled, so an increase of I_{DC} in one stage will make it slightly faster, thus shifting up the free-running frequency.

Given this topology, our degrees of freedom are the sizes of the Injector and Mixer transistors. For instance, to improve the locking range we have to scale down the Injector to lower the parasitics, thus increasing the injection efficiency. This improvement is diminished by the onset of short channel effects. The tail node parasitic can also be cancelled by resonating with an inductor [Wu01], but this is not practical at sub-GHz frequencies. We can also increase

	5-stage (div-8) @ 1 GHz	3-stage (div-4) @ 2.8 GHz
THEORY	**9%**	**34%**
SIMULATION	**5%**	**17%**
TEST	**2%**	**2%**

Table 4-2: Locking range comparison of 3-stage and 5-stage ring oscillator injection-locked frequency dividers.

the output swing and the W/L ratio of the Injector, hence increasing the swing ratio. This should be weighted against the resultant increase in parasitic capacitance and power dissipation.

A comparison of recently published data on low-power dividers is shown in Figure 4-10, where the present work is denoted by [0]. Power efficiency is defined as the ratio of the divider's maximum operation frequency to its power dissipation expressed in GHz/mW. As in [Vaucher00], to achieve a fair comparison of the available data, only the consumption of the "core" divider circuits is taken into consideration for calculating the power efficiency. The 5-stage ILFD achieves a power efficiency of 2.86 GHz/mW for a modulo-8 division at 1 GHz. The 3-stage modulo-4 divider achieves 2.82 GHz/mW at 2.8 GHz.

Finally, as expected, we observe that the phase noise of the divider tracks that of the injected signal source. When the oscillator is locked, the skirt of the frequency spectra as seen on the spectrum analyzer reduces significantly. Due to the limited locking range, the SSB phase noise measurements are too noisy to be accurate, so we cannot comment or draw any further conclusions from them.

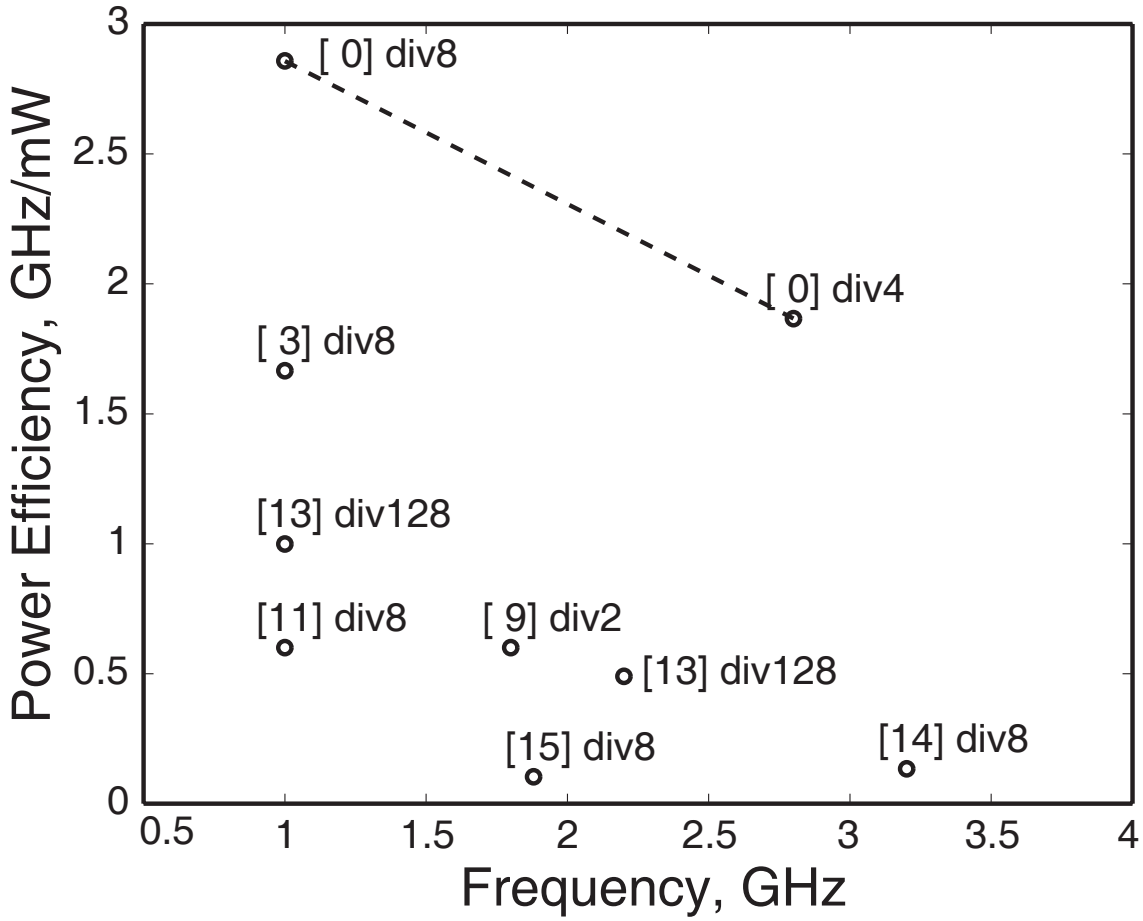

Figure 4-10 Comparison of power efficiency (GHz/mW) for different frequency dividers reported in the literature: [0] this work; [3] H. Darabi, A. Abidi, "A 4.5-mW 900-MHz CMOS receiver for wireless paging," *JSSC*, Aug. 2000; [9] H.R. Rategh and T.H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *JSSC*, Jun. 1999; [11] C.S. Vaucher, I. Ferencic, et. al, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-μm CMOS Technology," *JSSCC*, Jul. 2000; [13] Y. Kado, T. Ohno, et. al, "An Ultralow Power CMOS/SIMOX Programmable Counter LSI," *JSSC*, Oct. 1997; [14] Y. Kado, Y. Okazaki, et. al, "3.2-GHz, 0.2-μm Gate CMOS 1/8 Dynamic Frequency Divider," *Elec. Letters*, Sep. 1990; [15] J. Craninckx, M. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7-μm CMOS," *JSSCC*, Jul. 1996.

4.5 Summary

Ring oscillators are compact, require no external components, and can operate at very low power levels at sub-GHz frequencies. Moreover, every buffer in the ring oscillator ILFD operates at ω_0, which lowers overall power dissipation.

While a flip-flop based divider uses more power as we add more stages,

the injection-locked divider does not require more stages and furthermore uses less power for higher division ratios where every stage is operating at ω_0. In fact, as we have shown earlier (4-8), a smaller number of stages increases the locking range, making practical division ratios greater than two. In theory, a single-stage LC oscillator is capable of even lower power operation, but the large area required to integrate the inductors makes this choice impractical for sub-GHz operation. Resorting to off-chip inductors would compromise our goal of complete integration.

In this Chapter, we proposed a technique that has the potential of reducing power dissipation of frequency division by up to an order of magnitude compared to conventional digital approaches. We exploit injection-locking using differential CMOS ring oscillators for frequency division at 1 GHz and 2.8 GHz. We also present a simplified model of the injection-locked frequency divider (ILFD) that helps predict the locking range, and that also yields design insights that enable further optimization. These techniques enable the fabrication of a 1-GHz modulo-8 prescaler with the highest power efficiency (2.86 GHz/mW), in a 0.24-μm CMOS standard digital process.

There are still some questions that need to be answered before injection locked ring oscillators become a common idiom in RFIC design. A major limitation of these circuits is their severely limited locking range for high division ratios. Another limitation is the need for center frequency tunning of the ring oscillators over process, supply voltage, and temperature (PVT) corners for robust, high yield designs. Increasing both the locking and tuning range of ring oscillator injection-locked frequency dividers is the topic of Chapter 5.

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Chapter 5

The Injection-locked Loop

5.1 Introduction

In this chapter we report the development of the injection-locked loop (ILL), which extends the locking range of the injection-locked ring oscillator. The ILL exploits the extra phase that is introduced by injection mechanism as a detectable error in quadrature. This error, which is proportional to the deviation of the injected signal from the free running frequency of the oscillator, can be used in a feedback loop to adjust the oscillator closer to the injected signal's frequency, thus extending the locking range.

5.2 Motivation

Chapter 4's presentation of experiments with injection-locked ring oscillator frequency dividers show that large modulus division comes at the expense of a very limited operating range. Table 4-2 illustrates that the locking range is very limited for high order moduli. This shows that a major limitation of these circuits is their severely limited locking range for high division ratios. In order for the application of higher order moduli to be useful and practical, there

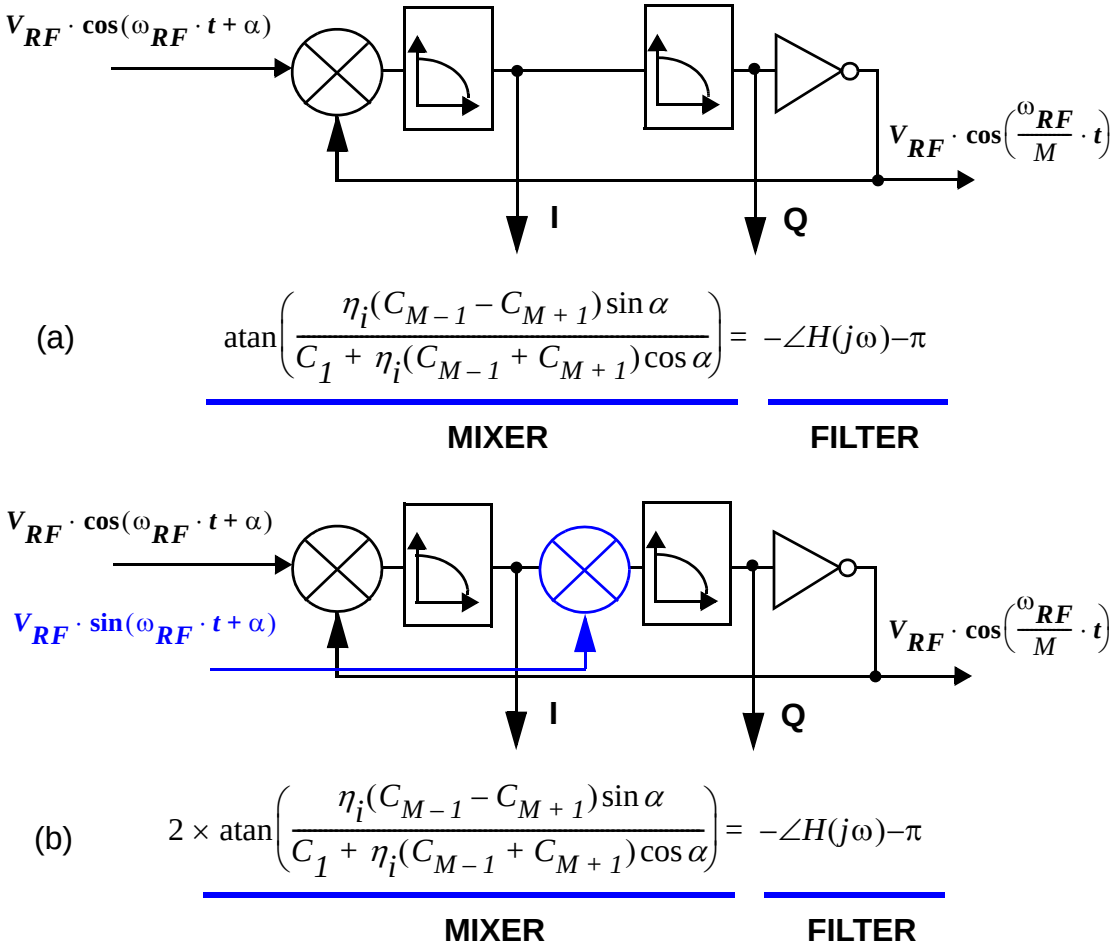

Figure 5-1 4-stage injection-locked ring oscillator: (a) using a single injector; (b) with quadrature injection

is a need for a mechanism that extends the locking range of the ring oscillator divider. Moreover, ring oscillators, by their very nature, are not very stable over process, temperature, and supply voltage (PVT) corners. This highlights another limitation, which is the need for center frequency tuning of the ring oscillators over PVT corners for robust, high yield designs. These observations lead to two fundamental research questions:

- How do we extend the locking range of the injection-locked frequency divider?
- How do we stabilize its free-running frequency over PVT corners?

5.3 Evolution of the Injection-locked Loop

5.3.1 Quadrature Injection

One way to increase the locking range is to use quadrature injection. As observed in Chapter 4, the locking range is limited by the maximum phase contribution of the mixer. One way to increase the locking range is to increase the phase contribution of the mixer. That can be accomplished by using multiple injection ports and mixers to increase the adjustment range. As shown in Figure 5-1, the locking range is almost doubled (in simulation) for two mixers. This scheme has two shortcomings: it requires multiple phases of the injected signal, and it is sensitive to the phase mismatch of the injected signals [Yue04]. Recent applications of this technique to quadrature-phase (i.e., I & Q) generators are presented in [Maligeorgos00] and [Chung04]. The structure is similar to that of a 2-stage ring oscillator with quadrature injection using two mixers. Although the authors claim a quadrature error of less than 1°, this circuit requires manual adjustment of the mixer bias currents in order to null the quadrature error due to device mismatches and the injection mechanism itself.

5.3.2 Injection-locked PLL

Uzunoglu and White's paper [Uzunoglu85] described the basis for *synchronous oscillators*. The authors use Adler's theory to analyze a discrete implementation of an injection-locked Colpitts oscillator, and describe its application to carrier and clock recovery circuits in QPSK modems. In 1989 they introduced the coherent phase-locked synchronous oscillator (CPSO) which adds a phase tracking loop to the synchronous oscillator to extend its locking range [Uzunoglu89]. As discussed in Section 2.2.2, Adler had shown that the steady state phase between the injection-locked oscillator and the injected signal is a function of the frequency difference between the free running oscillation and

the injected signal. While locked, a phase difference of anywhere from $-\pi/2$ to $\pi/2$ exists between these signals. Moreover, a zero-degree phase shift occurs at the center of the locking range. The CPSO detects this phase relationship using a mixer and uses the phase error to tune the oscillator's free-running frequency to the center of the locking range. A more recent example of this technique is found in [Chang99] as illustrated in Figure 5-2(b).

Even though we know that we can use the phase difference between input and output of an injection-locked system for frequency tracking, it is not practical to do so if the output is at a different frequency from the input. This drawback reduces the usefulness of this technique for harmonically-locked systems such as frequency dividers where the input and output frequencies differ.

5.3.3 Harmonic IL-PLL

A technique that counteracts the disadvantage of the IL-PLL is the harmonic injection-locked PLL presented in [Kudsuz'00] for a harmonically-locked frequency multiplier. In this scheme, the multiplied output frequency is down-converted with a mixer before its phase is compared with the injected signal. The inverse case for a frequency divider is presented in Figure 5-2(c). It requires generating a harmonic of the output to compare with the injected signal. Direct phase detection thus require a second path of frequency conversion, which makes it very cumbersome and inefficient, especially if we care about power dissipation. In theory, a sampling phase detector could be used, but further processing at the (higher) input injection frequency would still be required. Having additional high-frequency circuit overhead negates the power savings of the ILFD at large moduli. The fundamental question still remains: How can we extract the phase information using simple, power efficient circuits?

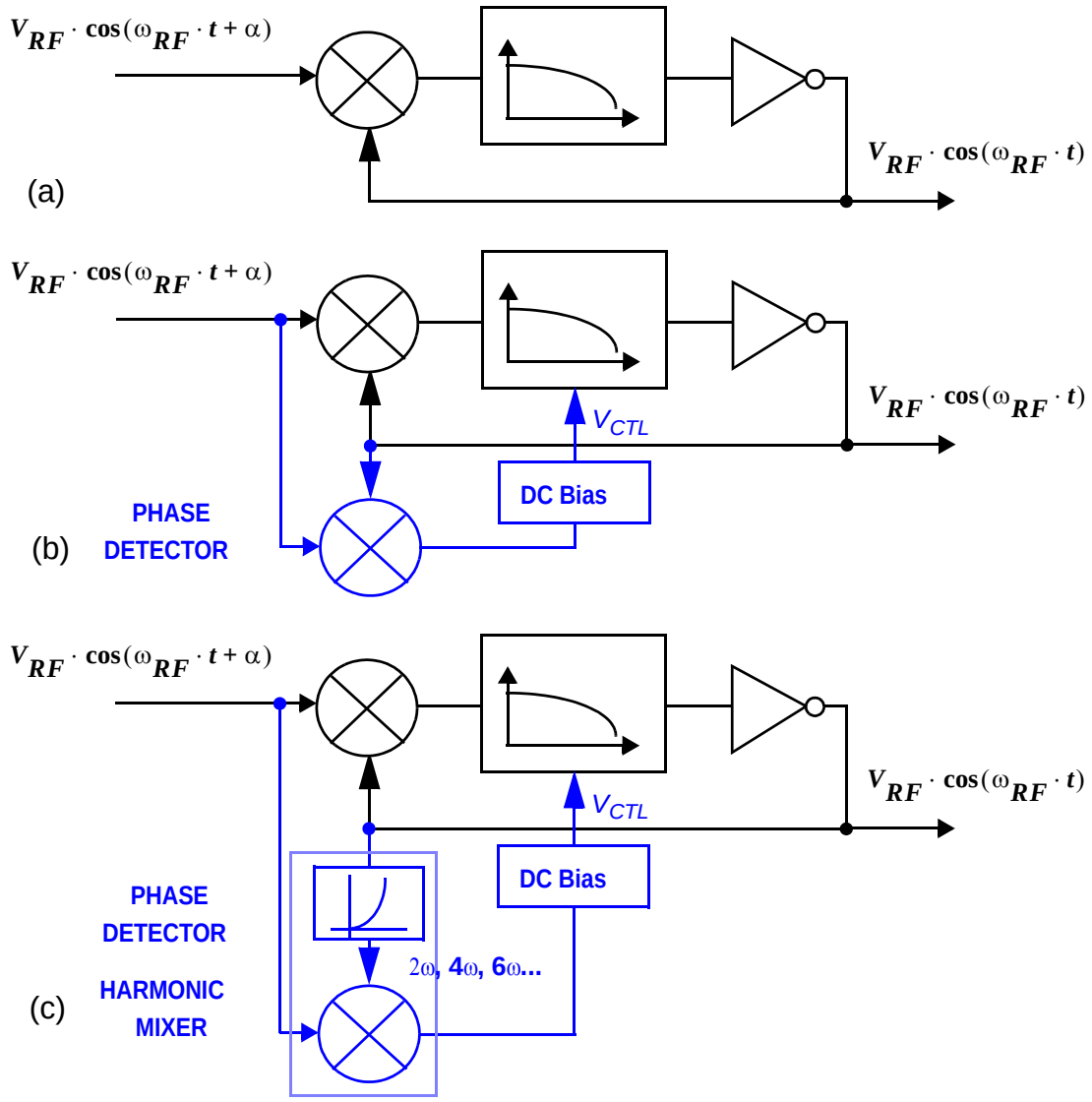

Figure 5-2 Techniques for extending the locking-range: (a) Miller divider; (b) Injection-locked PLL [Chang99]; (c) Harmonic IL-PLL [Kudszus00]

5.3.4 Injection-locked Loop

Our previous work with 4-stage injection-locked differential ring oscillators (Chapter 4) sets the stage for an interesting observation: the extra phase that synchronizes the oscillator to the injected signal is detectable as an error in quadrature. Moreover, this error is proportional to the deviation of the injected signal from the free running frequency of the oscillator. Furthermore, this error can be used in a feedback loop to adjust the oscillator closer to the

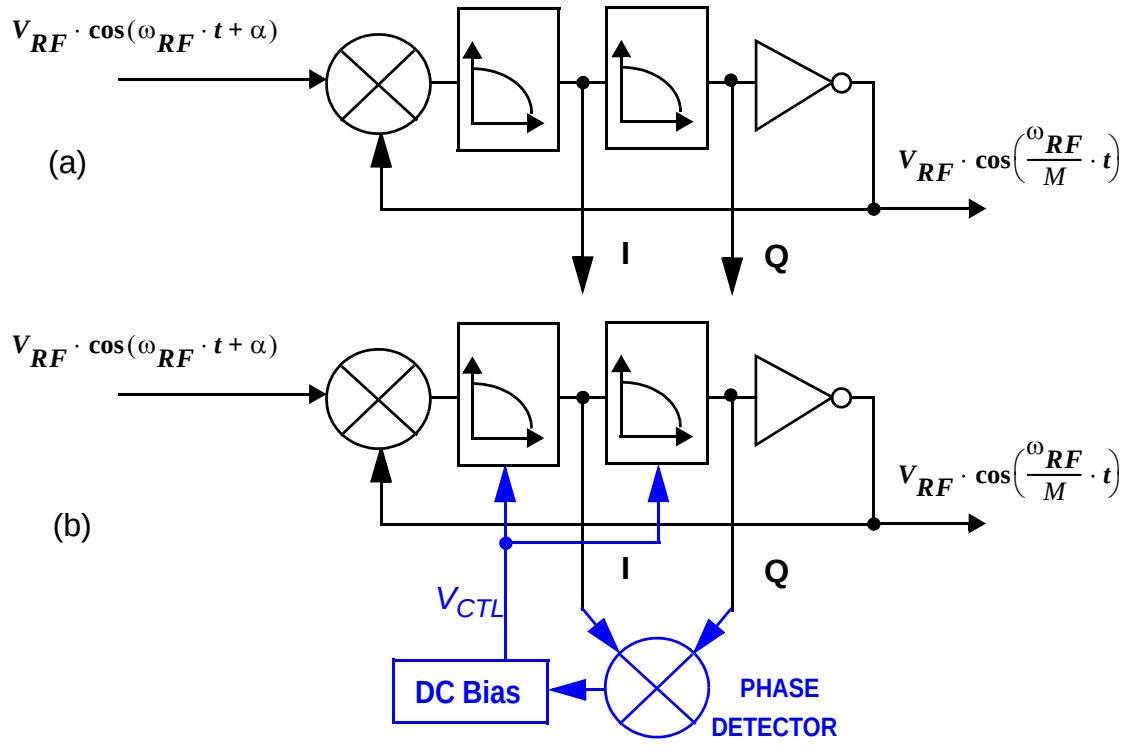

Figure 5-3 Evolution of the injection-locked loop: (a) Miller model for a 4-stage injection-locked ring oscillator; (b) Injection-locked quadrature tracking loop

injected signal's frequency, thus extending the locking range. This is a key observation, as we can implement a tracking loop that operates with signals at the *lower* output frequency, thus having minimal impact on power dissipation. Figure 5-3(b) shows the basic block diagram for the injection-locked loop (ILL). In the ILL, the quadrature phase error is detected using a mixer and that information is used to adjust the bias of the ring oscillator. This tunes the oscillator's free-running frequency to the center of the locking range. An exhaustive search of the literature does not produce a single report of this technique.

There are many advantages to the injection-locked loop. First, because it adjusts with the injected signal frequency, it is tolerant to variations in injected frequency, fabrication process, and temperature drift. Second, the quadrature detection mixer operates at the lower output frequency, thus

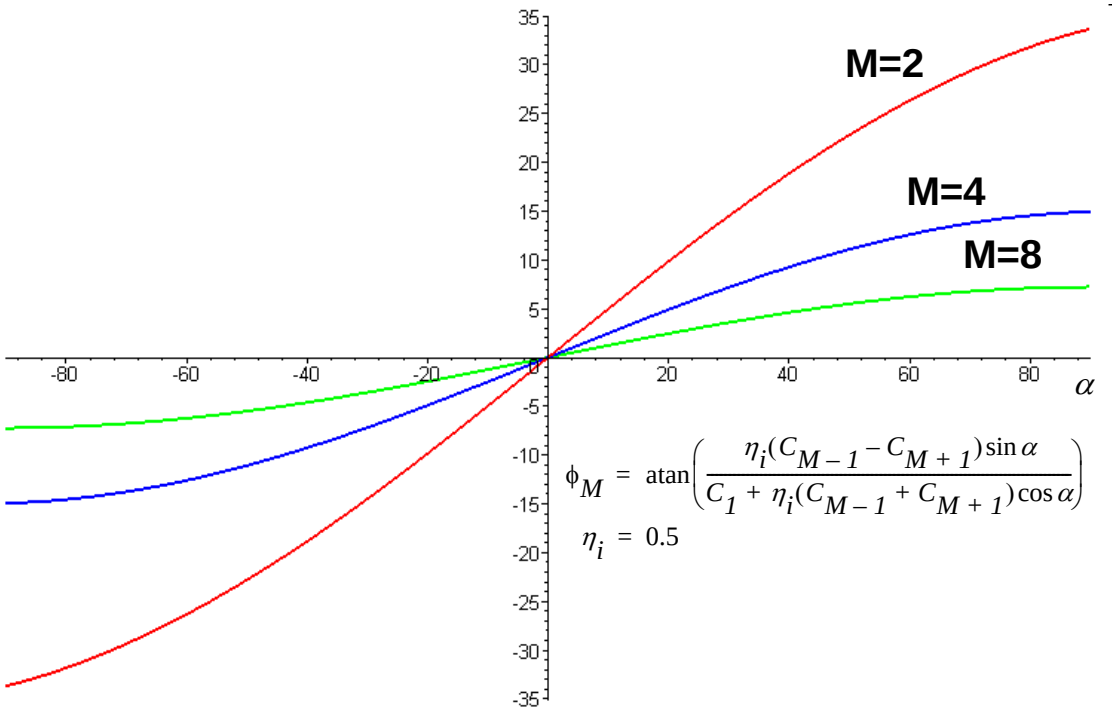

Figure 5-4 Phase contribution of the mixer

minimizing the power dissipation of the components of the feedback loop. Third, the quadrature error of the outputs is minimized by the tracking loop, thus making it useful for quadrature (I & Q) generators. Fourth, the fact that the oscillator's free-running frequency tracks the center of the locking range maximizes the transient response and the phase noise filtering properties of the circuit. Finally, the ILL can be easily integrated using simple, well understood analog building blocks. Section 5.4 describes the modeling of the injection-locked loop.

5.4 Modeling of the Injection-locked Loop

Chapter 4 establishes that the injection mixer contributes additional phase which is a function of α, the frequency difference between the free running oscillation and the injected signal. We also know from experience that this additional phase causes an error in quadrature in a 4-stage ring oscillator.

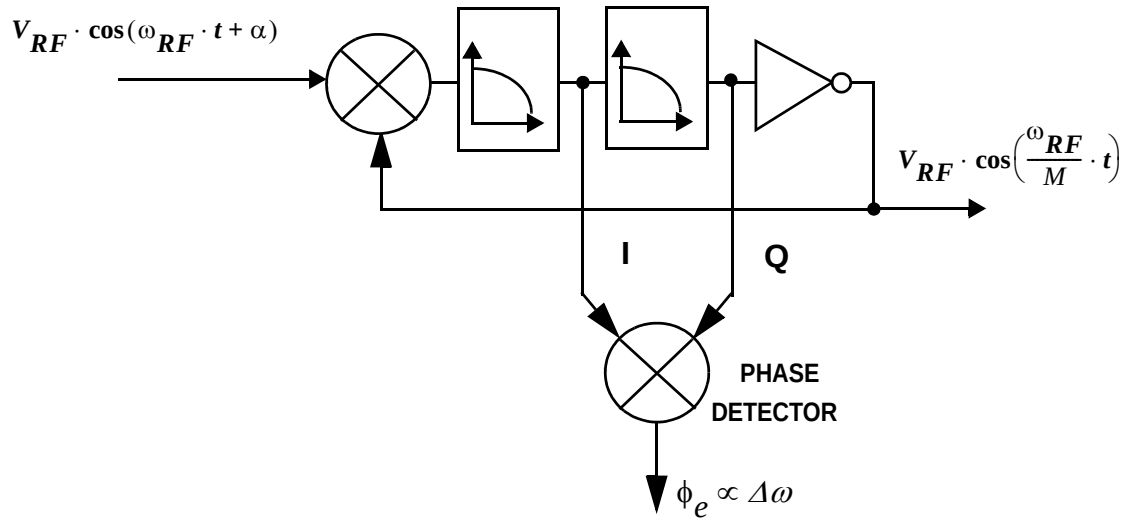

Figure 5-5 Evolution of the injection-locked loop: phase contribution of the filter

To model the phase detection mechanism first we need to determine how the injection mixer contributes to the phase quadrature error. We know that this mixer contributes a phase shift to the loop which is a monotonic function of α as shown in Equation (5-1).

$$\text{atan}\left(\frac{\eta_i(C_{M-1} - C_{M+1})\sin\alpha}{C_1 + \eta_i(C_{M-1} + C_{M+1})\cos\alpha}\right) = \angle H(j\omega) - \pi \ . \tag{5-1}$$

In this expression, we observe that zero phase is added when the injection frequency is at the center of the locking range. Figure 5-4 plots the phase contribution of the injection mixer for different division ratios, *M*. From this plot, we can observe that the range of phase adjustment is limited at higher division ratios. Moreover, if the system is frequency locked, the excess phase of the injection mixer reduces the phase contribution of the filter stages. Given that each filter stage contributes a maximum of $\pi/4$ to the loop phase, we can deduce the following expression for the excess phase of the injection mixer, ϕ_M.

$$\phi_M = -\angle H(j\omega) - \pi \tag{5-2}$$

$$\text{and } \phi_M \cong 2 \cdot \frac{\Delta\omega}{\omega_N}, \tag{5-3}$$

$$\text{where } \Delta\omega = \omega - \omega_N \ . \tag{5-4}$$

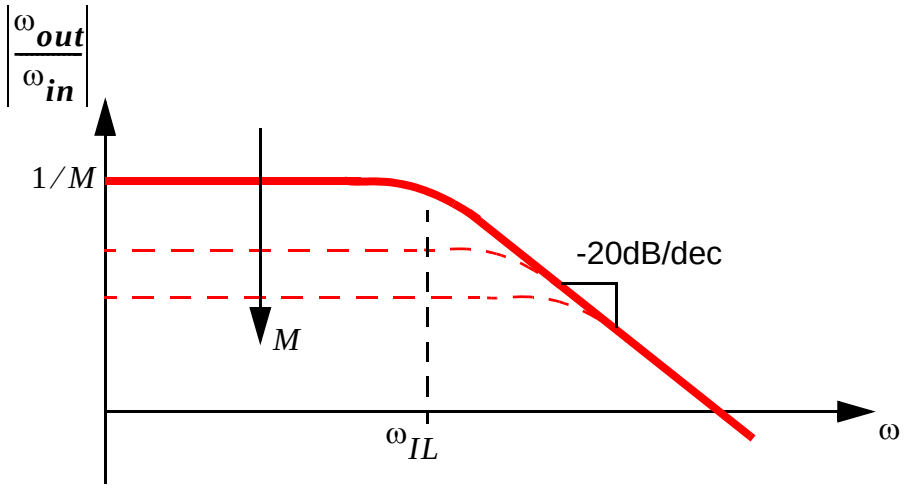

Figure 5-6 Transient response of the injection-locked loop

We observe that the excess mixer phase is proportional to the deviation from the free-running frequency, demonstrating that the error in quadrature is proportional to the deviation from the center of the locking range. This excess phase also reduces the filter phase contribution by $\phi_M/4$. Hence, a phase detector placed between the quadrature (I & Q) outputs of the ring oscillator can be used to extract an error signal proportional to ϕ_M as shown in Figure 5-5.

Also from Chapter 4, as illustrated in Figure 5-6, we know that the transient response of the injection-locked divider is that of a 1st-order system [Rategh99] and is given by

$$\frac{\omega_{out}}{\omega_{in}} = \frac{1/M}{\left(1 + j\frac{\omega}{\omega_{IL}}\right)} \tag{5-5}$$

$$\text{and } \omega_{IL} \cong M \cdot \left|\frac{k_0}{S}\right|, \tag{5-6}$$

where the pole frequency ω_{IL} is given by the same parameters that affect the locking range such as division ratio and injection efficiency [Verma03]. Therefore, the maximum input tracking bandwidth is achieved when the free-running frequency is centered within the locking range.

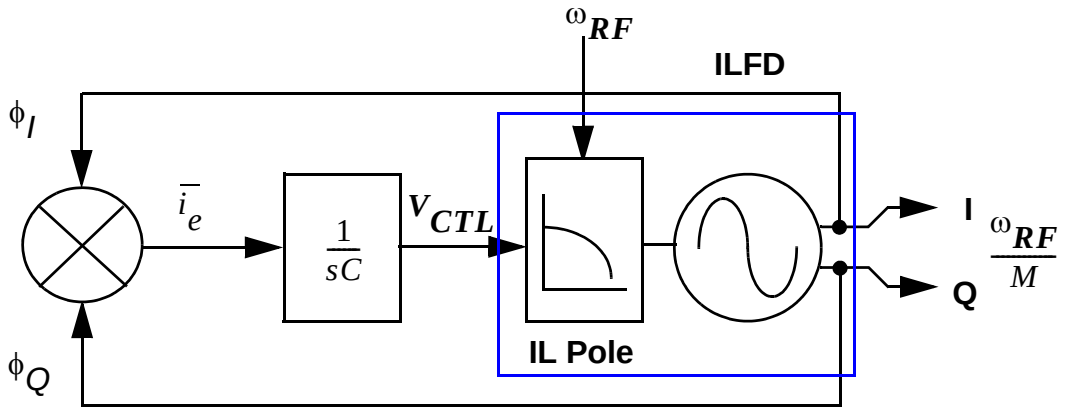

Figure 5-7 Linearized model of the injection-locked loop

Using this information, and assuming a simple integral controller, we propose the LTI model for a phase tracking control loop shown in Figure 5-7. In this model, the mixer outputs a current proportional to the deviation from quadrature of the I & Q outputs of the oscillator. This current is integrated into V_{CTL} by a loop filter capacitor, and used to adjust the free-running frequency of the ILFD. To model the effect of the ILFD's bias adjustment on the ILL's loop dynamics, we need to determine the phase transfer function of the ILFD as a function of V_{CTL}. In practice, a locked oscillator cannot distinguish a small step V_{CTL} from an equivalent step in the injected frequency[1]. Therefore, we assume that a small step in V_{CTL} is equivalent to an input frequency step of $MK_V V_{CTL}$ for a modulo-M ILFD[2], where K_V is the VCO's voltage to frequency transfer characteristic. Consequently, to complete the model for the ILL, we use a single pole at ω_{IL} to model the phase response of the ILFD to V_{CTL}.

1. We implicitly assume that the locked oscillator will respond to a small change in V_{CTL} instantaneously, thus neglecting the dynamics in the frequency tuning path. For most ring oscillators this assumption is very reasonable.
2. This assumption can also be shown analytically, whereas for a small step in V_{CTL}, the phase response can be approximated by the same 1st order differential equation as derived by [Rategh99] for a small step in phase of the injected signal.

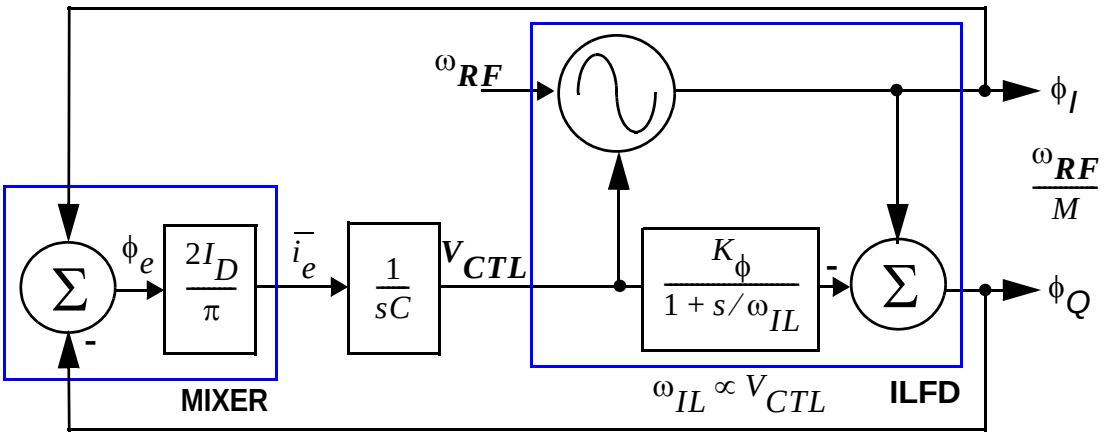

Figure 5-8 Linearized model of the injection-locked loop (detailed)

Furthermore, we assume that ω_{IL} is constant for a small disturbance in V_{CTL}.

Finally, a more detailed model of the ILL is shown in Figure 5-8. While the injection locking mechanism of the ILFD maintains frequency synchronization with ω_{RF}, the mixer acts as a phase detector, where the error in quadrature is proportional to deviation from the center of the locking range. The phase detector gain is given by $2I_D/\pi$, and again, the I & Q phase error is extracted from the DC component of the mixer's output using an integrator ($1/sC$) to generate V_{CTL}. Once more, we add a pole at ω_{IL} to model the ILFD's response to a change in V_{CTL}. This leads to a second order, type-I feedback system with open loop gain described by Equation (5-7):

$$L(s) = \frac{2I_D \cdot K_\phi / \pi C}{s(1 + s/\omega_{IL})}, \tag{5-7}$$

where the phase shift constant $K\phi$ given in radians/volt. The root locus of this equation is plotted in Figure 5-9 and shows that the ILL is always stable. The single integrator guarantees that there is zero steady state error for a step input.

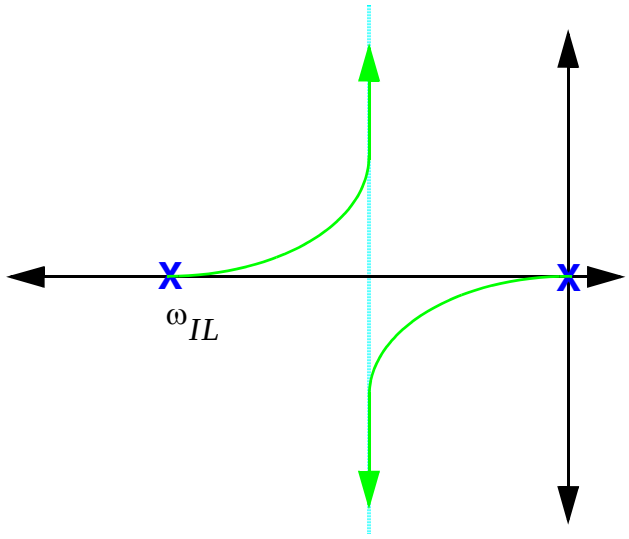

Figure 5-9 Root locus of the injection-locked loop

5.5 Circuit Implementation of the Injection-locked Loop

Figure 5-10 shows a block diagram of one possible implementation of the injection-locked loop. It consists of an injection-locked voltage-controlled ring oscillator (IL-VCO), an injector with bias compensation circuit (INJECTOR BIAS), a quadrature phase detector (MIXER), two loop filter capacitors (2C), and bias generator for the IL-VCO (VCO BIAS).

In operation, a differential double-balanced symmetric mixer with folded cascode output stage acts as a phase detector. The output of the mixer is a current proportional to the quadrature phase error and is integrated by the filter capacitors *2C* into *vcp* & *vcm*. The *Vctl* and *Vref* inputs of VCOBIAS are used for coarse tuning of the free-running frequency ω_N, while the filtered outputs *vcp* and *vcm* fine tune ω_N. The injector BIAS block generates bias voltage for the VCO's injector stage and compensates for the increase in I_{DC} due to tail device non-linearity (see Section 4.4). The rest of this section describes the circuit building blocks used in the ILL.

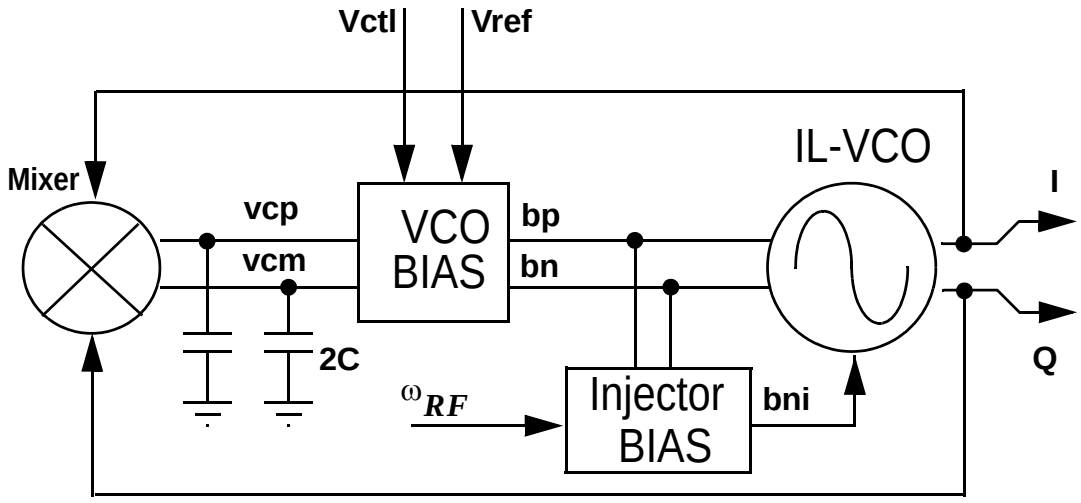

Figure 5-10 Block diagram of the injection-locked loop

5.5.1 Injection-locked Voltage-Controlled Ring Oscillator

In this embodiment, the ILL uses a 4-stage differential ring oscillator to generate quadrature phases I & Q (Figure 5-11). The oscillator uses symmetric-load buffer stages for good supply noise rejection (see Section 3.2.3). Buffer **B1** is used as the injection mixer and has a separate injection port *bni* to bias the tail of its differential pair. A buffer replica is used to set the symmetric-load bias voltage *bp*. All outputs are buffered to minimize phase offsets due to loading of the stages.

To tune the IL-VCO's free running frequency, ω_N, we propose the linearized transconductor shown in Figure 5-12. The total bias current is given by

$$\Delta I \cong I_1 + I_2 + \frac{\Delta Vctl}{R1} + \frac{\Delta vc}{R2}\ , \tag{5-8}$$

$$\Delta Vctl\ =\ Vctl - Vref\ , \tag{5-9}$$

$$\text{and } \Delta vc\ =\ vcp - vcm\ , \tag{5-10}$$

where I_1 and I_2 are the bias currents of the transconductors using $1/R1$ and $1/R2$ respectively. The second transconductor adds fine tuning current from the

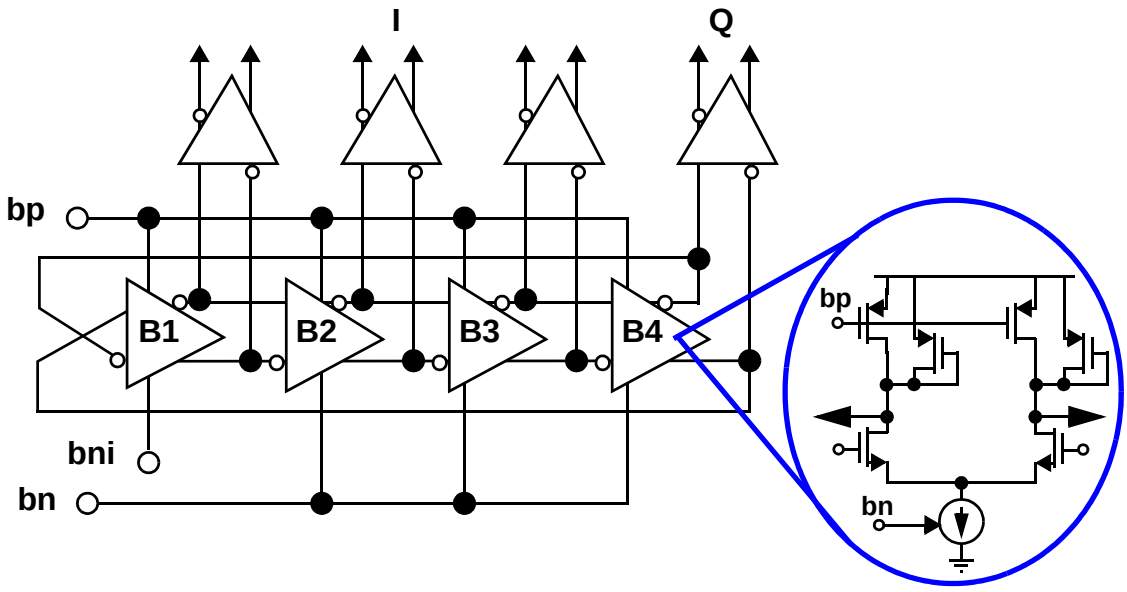

Figure 5-11 Voltage-controlled quadrature ring oscillator

phase detector/filter to close the phase tracking loop. Current ΔI flows into mirror transistor **MN1** to set the tail bias voltage *bn*. A buffer replica, **BR**, is used to set the symmetric-load bias voltage *bp*.

The injection stage needs a special bias block that compensates for tail device nonlinearity. In Section 4.4 we observe that strong injection disturbs the biasing and "pushes" the free-running frequency of the VCO. This is caused by an increase in I_{DC} due to tail device non-linearity in the injection stage. To compensate for this increase in tail current we propose the injector replica circuit shown in Figure 5-13. In this implementation, the injected current in the replica circuit (i'_{RF}) is filtered to extract an approximation to the DC component generated by the nonlinearity of **MN1**. This current is combined with the injected curent i_{RF} and the bias current I_b from the VCOBIAS circuit to generate the current $I_{out} = (I_b + i_{RF}) - I_{DC}$. This current then flows into mirror **MN2** to set the injector voltage *bni*.

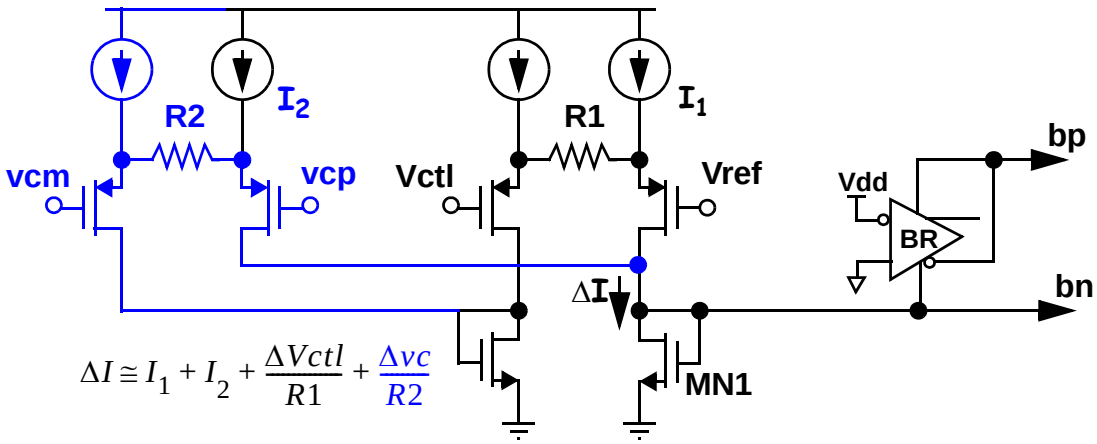

Figure 5-12 Bias tuning of ring oscillator

5.5.2 Quadrature Phase Detector

The quadrature phase detector uses a symmetric XOR as a mixer [Razavi94] as shown in Figure 5-14. The output stage is a differential folded cascode using wide-swing cascoded mirrors and a common-mode feedback (CM-FB) circuit that sets the common mode output voltage to $V_{cm} = V_{dd}/2$. When connected to the I & Q outputs of the IL-VCO, the average output current is proportional to the quadrature offset, ϕ_e. In operation, the output current ΔI flows into integrating capacitors 2C to generate $\Delta V = vcp - vcm$. The symmetric XOR mixer (Figure 5-15) is chosen because of its low phase error at high frequencies due to equal signal paths for I & Q. In contrast to a Gilbert multiplier, this circuit operates with a lower voltage headroom because there are no stacked transistors in the RF path. In operation, the reference voltage, vb, which equals the common-mode level of I & Q, is generated using a replica of the IL-VCO buffers.

The common-mode feedback circuit of Figure 5-16 is used to set the common-mode output voltage to $V_{cm} = V_{dd}/2$. This circuit is selected for simplicity over performance. Hence, the common-mode input range is quite restricted and

is limited by the threshold voltage of transistors **MN1** and **MN2**. Additional feedback capacitors **CFB** are required for loop compensation.

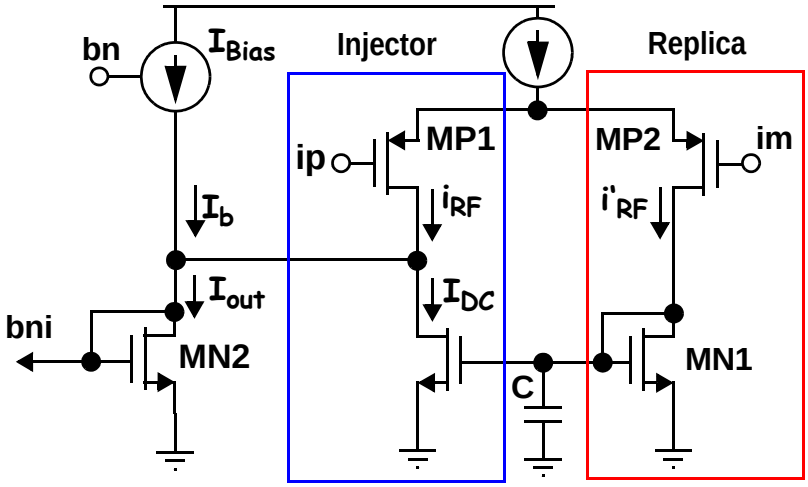

Figure 5-13 Bias compensation of injector

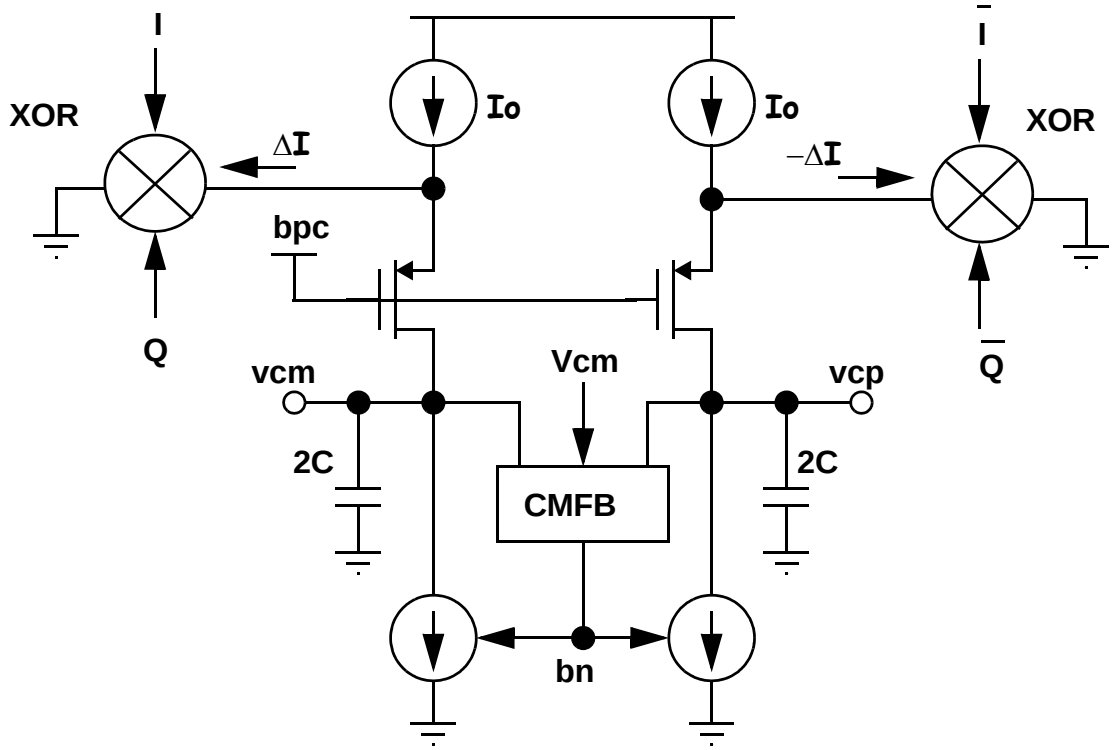

Figure 5-14 Quadrature phase detector and loop filter

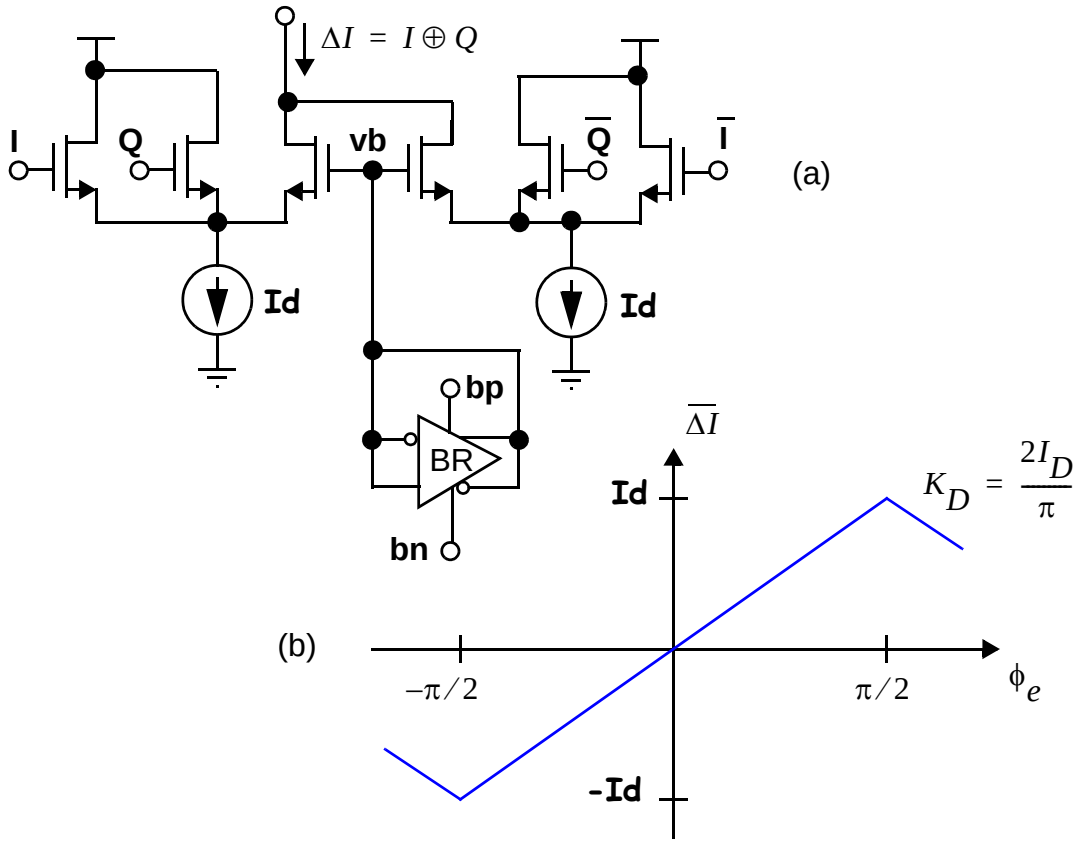

Figure 5-15 Symmetric XOR mixer [Razavi94]: (a) Simplified schematic diagram; (b) Mixer gain

5.6 Tuning of the Injection-locked Loop

In many applications, such as PLL frequency synthesis, enhancing the locking range with an ILL is not enough, as the ILFD needs to be locked in order for the ILL to track, i.e., the ILL requires a frequency acquisition aid to initialize the loop. Initial frequency acquisition of an ILFD to a VCO in a PLL is not a trivial task.

Previous work using injection-locked *LC* oscillators has been plagued by offset and gain mismatch in the voltage to frequency tuning characteristics of the oscillators [Rategh00]. Using ring oscillators is even worse, as the same control voltage needs to produce a different frequency in each of the oscillators. To illustrate this difficulty, lets use as an example the 1-GHz phase-locked loop

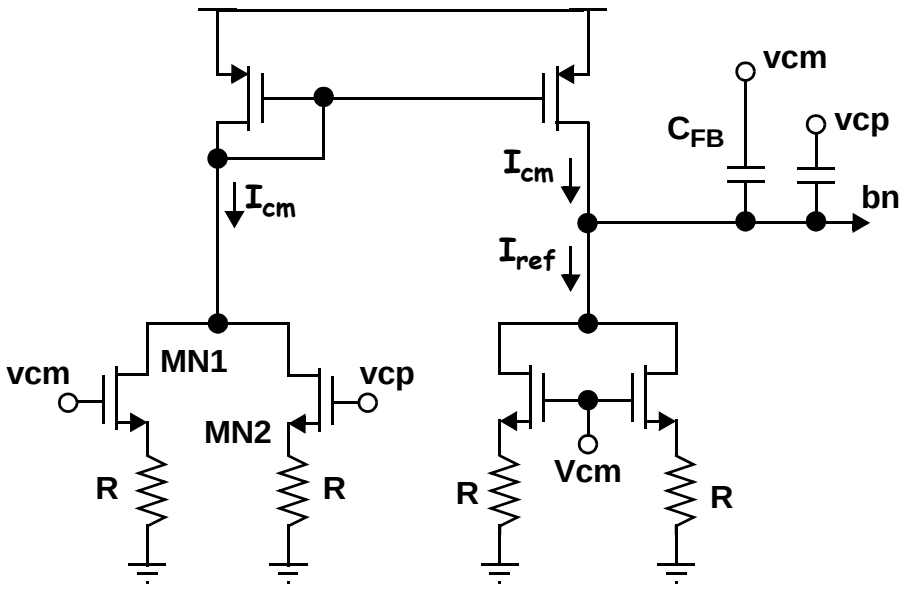

Figure 5-16 Common-mode feedback circuit for phase detector

of Figure 5-17, where a modulo-4 ILFD needs to track the VCO. This is a third order, type-II system[3]. Let's assume that both the ILFD and VCO are based on a ring oscillator topology. The ILFD is used as a prescaler to save power. The ILL extends the ILFD's locking range and minimizes its phase noise contribution to the PLL.

In this example, unless the bias circuits are exceptionally stable, the tuning gain of the ILFD should be compensated to be about *1/4* the gain of the VCO. It is necessary for the VCO's frequency always to be within the "natural" locking range of the ILFD over PVT corners, at least initially, while the ILL adjusts the ILFD center frequency (i.e., during ILL frequency acquisition)[4]. However, a ring oscillator's gain is typically ill-controlled over PVT corners, e.g., a factor of two of variation is not uncommon. Also, the tuning characteristic is usually not linear but can best be described by a cubic spline. In consequence, for frequencies that are two octaves apart (as is the case for this example), the

3. See Appendix 5.9 for a simple PLL design recipe.
4. Once the ILL is locked, this restriction can be removed.

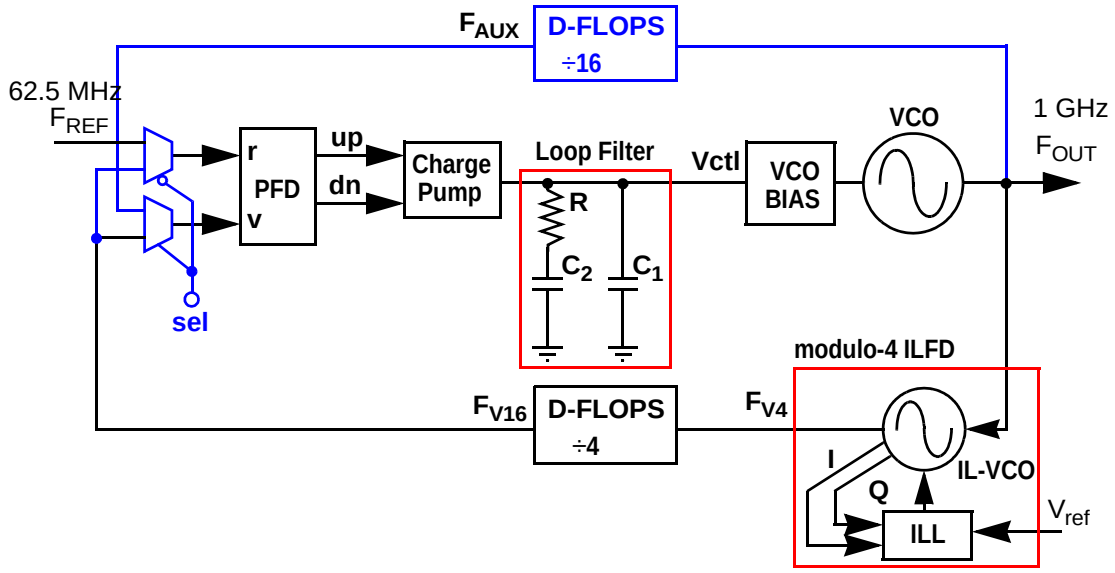

Figure 5-17 ILL prescaler for 1-GHz PLL frequency synthesizer

slope of the curve (i.e. "gain") changes significantly. This is complicated even further by the fact that in a PLL the VCO's frequency changes as the loop acquires lock.

Clearly, just matching (or linearly scaling) the two oscillators is not enough. One possible solution is to use a calibration scheme in which both the slope and offset of the tuning curve are adjusted. The main drawback of this scheme is that it requires a complex calibration procedure because the frequency has to be measured at least twice for the VCO and ILFD separately. This is cumbersome and not very practical. Therefore, trying to match the tuning characteristic of the ILFD with that of the VCO is not a good approach.

Our proposed approach uses the components shown in blue. In this scheme, we turn the problem around. Instead of adjusting the tuning characteristic of the ILFD to track that of the VCO, we use the same PLL to force the VCO to lock to the ILFD. This is illustrated in Figure 5-18.

The first step, shown in Figure 5-18(a), is to close the loop using an

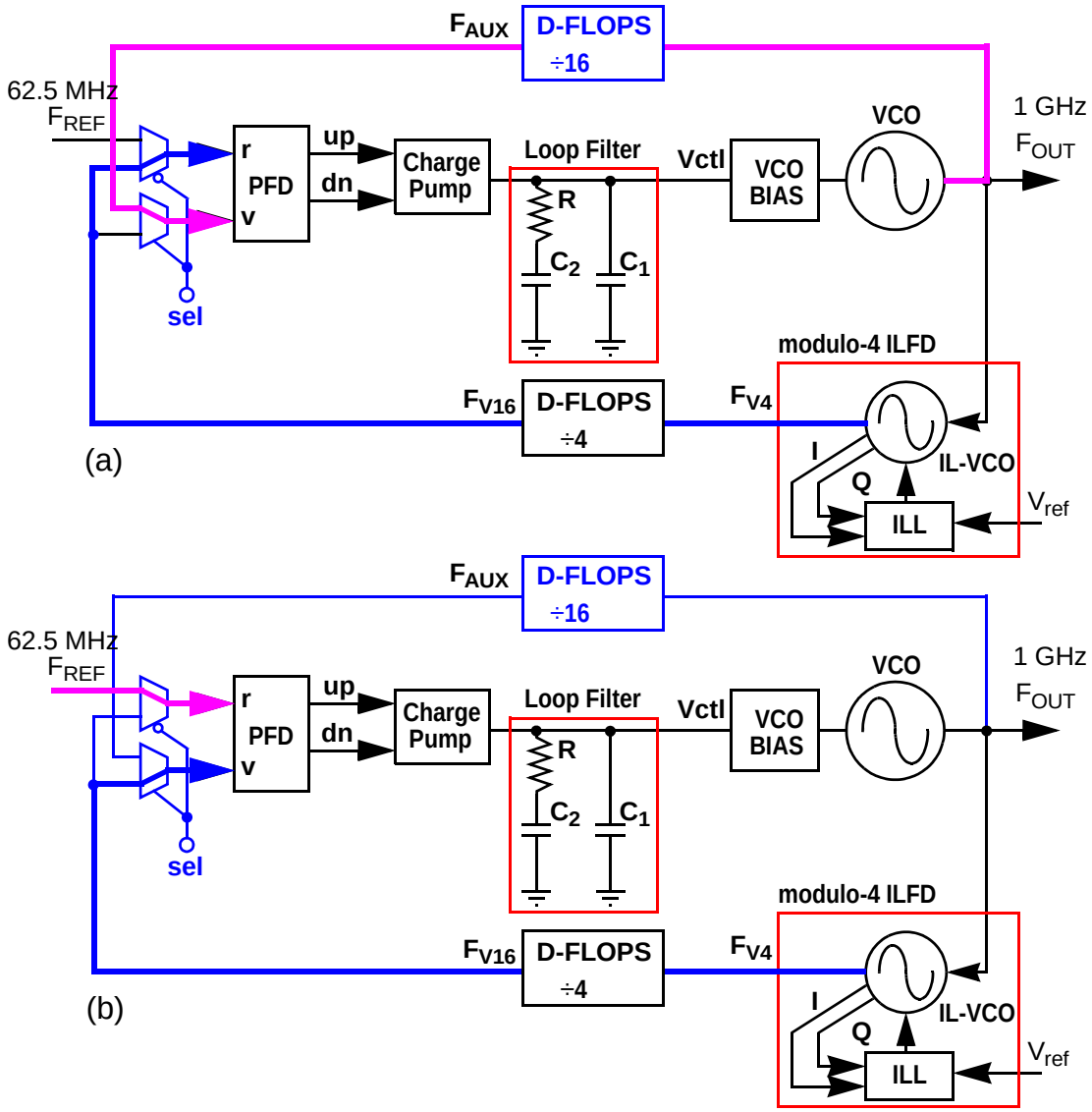

Figure 5-18 Tuning of the ILL: (a) Calibration phase; (b) Locking phase

auxiliary modulo-16 divider for the feedback path (v) and the ILFD as the source for the frequency reference (r). After settling, the PLL will have forced the VCO's frequency to be at a precise harmonic of the ILFD (the 4^{th} harmonic, in this case). In step two, shown in Figure 5-18(b), we switch the reference to an external source, turn off the auxiliary divider, and turn on the injection to the ILFD. Because the VCO is precisely centered at a harmonic of the ILFD, locking will occur very quickly, within a cycle or two[5]. Any glitches will be

filtered by the much lower bandwidth of the PLL[6]. Finally, both the VCO and ILFD will eventually settle to their final frequencies dictated by the external reference. Meanwhile, the ILL will adjust the biasing of the ILFD to track the VCO.

5.7 Experimental Verification

5.7.1 Design of a 1-GHz Quadrature Generator Test Chip

To test the operation of the injection-locked loop, consider a precise quadrature generator test chip designed using National Semiconductor's 0.24μm CMOS8 process (Figure 5-19). This test chip integrates a master **VCO**, injection-locked slave **VCO**, frequency-doubling injector, and differential quadrature phase detector (PD mixer). The master **PLL** is implemented externally to facilitate testing, and a test mixer is used to measure quadrature phase error.

In operation, the signal from the master VCO is injected into a frequency doubler whose output feeds into a modulo-2 injection-locked 4-stage ring oscillator frequency divider (ILFD). The ILFD is a replica of the master VCO and both operate at the same frequency. Doubling the frequency before injecting into the slave also allows using identical replicas for the oscillators, thereby enabling the use of the master's V_{CTL} to coarse-tune the injection-locked slave. The ILL corrects the quadrature error of ring oscillator and relaxes the offset and mismatch requirements of the oscillator buffer stages. The tracking behavior of the ILL also maximizes the locking range, thus minimizing the phase noise contribution of the quadrature generator.

---

5. This assumes that the natural locking bandwidth of the ILFD (IL-BW) is much greater than the PLL's closed-loop bandwidth (PLL-BW).
6. Assuming that the ILL-BW, albeit lower than the IL-BW is also greater than the PLL-BW.

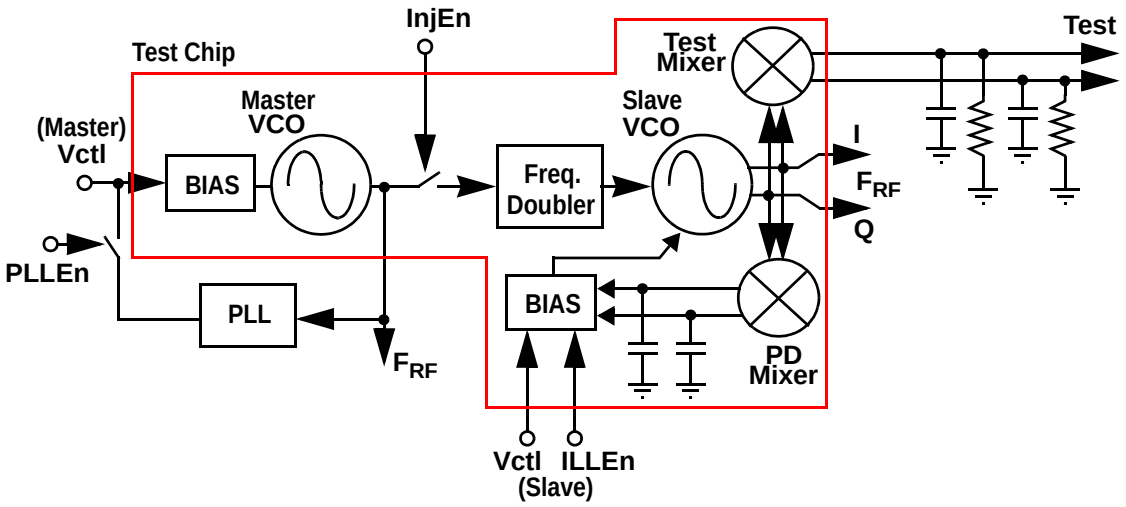

Figure 5-19 1-GHz quadrature generator ILL test chip

The diagram for the injector and frequency doubler circuit used in the test chip is shown in Figure 5-20. Transistors **MP1 & MP2** perform frequency doubling and an injector replica circuit is used to compensate for the increase in DC bias current due to tail device non-linearity in the injection stage. As shown earlier (Section 5.5.1, Figure 5-13), the injected current in the replica circuit (i'_{RF}) is filtered to extract the DC component due to the nonlinearity of **MN1**. This current is combined with the injected curent i_{RF} and the bias current I_b from the VCOBIAS circuit to generate the current $I_{out} = (I_b + i_{RF}) - I_{DC}$. This current then flows into mirror **MN2** to set the injector voltage *bni*. Both mixers are implemented using the circuit described in Section 5.5.2, Figure 5-14. The VCO bias circuit is the same one shown in Figure 5-12.

5.7.2 Measurement Results

The test chip whose micrograph is shown in Figure 5-21 is fabricated using National Semiconductors 0.24μm CMOS8 process (2-poly/5-metal). The chip is pad-limited with die area of $1mm^2$, with an active area of less than $0.15mm^2$.

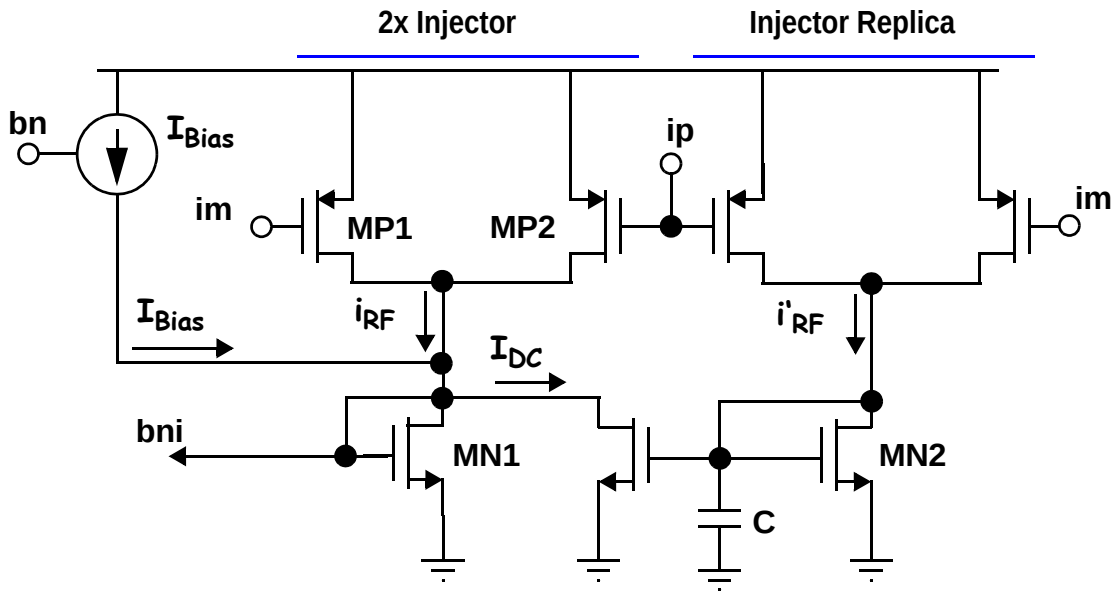

Figure 5-20 Test chip: Frequency-doubling injector

The master and slave VCOs' tuning characteristics are well matched to each other and also close to what was expected from simulation (see Figures 5-22 & 5-23). The master VCO's gain is 465-507MHz/V with an offset of 1,104 to 1,222MHz. The slave VCO's gain is 467-565MHz/V with offset of 1,160 to 1,323MHz.

Both the master's and the slave's output amplitudes are smaller than expected. The output buffers are designed for 0dBm, but measured output levels are -20dBm. This discrepancy may be due to severe losses in the FR-4 PCB used for test, baluns, and connectors.

With injection enabled, the locking range is also significantly smaller than expected. Specifically, the design goal is a 120MHz locking range for 1-GHz injection, as verified using ADS (TekSpice) simulations. More recent simulations using Cadence's Spectre show that the locking range is less than 20MHz, which is close to what was verified experimentally.

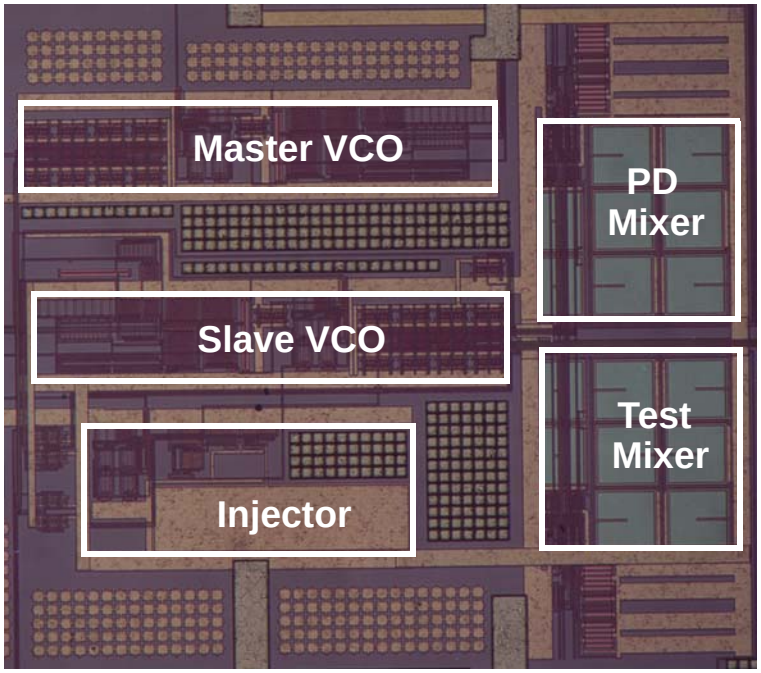

Figure 5-21 Test chip micrograph

Testing also uncovered a rather large DC offset at the output of the test mixer due to a layout error. The resistors in the mixers' CMFB circuit are laid out with a width of only 0.24μm introducing a mismatch of up to 20%. These resistors should have been laid out at least 2μm wide to achieve 1% or better matching. This error was corrected in a second revision of the test chip.

Testing of the injection-locked loop was unsuccesful, because when activated, the ILL drifts immediately towards the power supply rail and is unable to track. We believe that this problem is due to resistor layout mismatches that introduce a substantial differential offset at the mixer's output. This offset exceeds the maximum adjustment range of the fine-tuning transconductor in the slave's bias circuit, causing the loop to rail. This layout error was fixed along with other layout enhancements to improve the matching of the filter capacitors. The second version of the test chip was taped out and fabricated on November 2003. Unfortunately**,** lack of time prevented testing of the second spin.

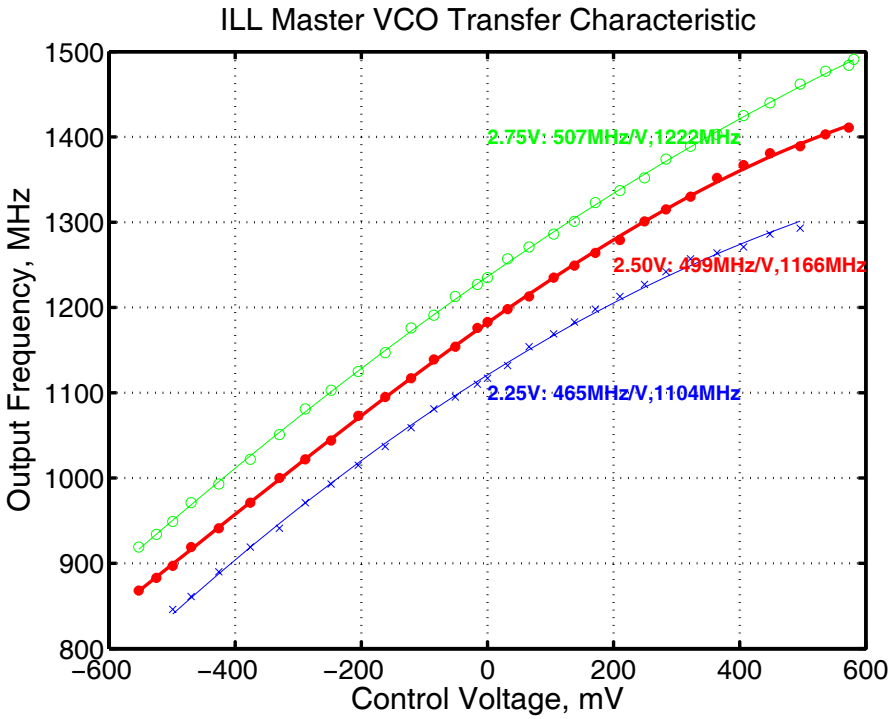

Figure 5-22 ILL Master VCO transfer characteristic

5.8 Summary

This chapter has discussed the developmnet of the injection-locked loop, which extends the locking range of the injection-locked ring oscillator frequency divider. The ILL exploits a property of injection-locked oscillators, where the extra phase introduced by injection in 4-stage differential CMOS ring oscillators is detectable as a quadrature error which is proportional to the deviation of the injected signal from the free running frequency of the oscillator.

.Our experience with ring oscillator frequency dividers reveals that large modulus division comes at the expense of a very limited operating locking range. In order for higher order moduli to be useful and practical, we have developed a technique to extend the locking range of the injection-locked frequency divider. We discussed the concept of the ILL and described the evolution that

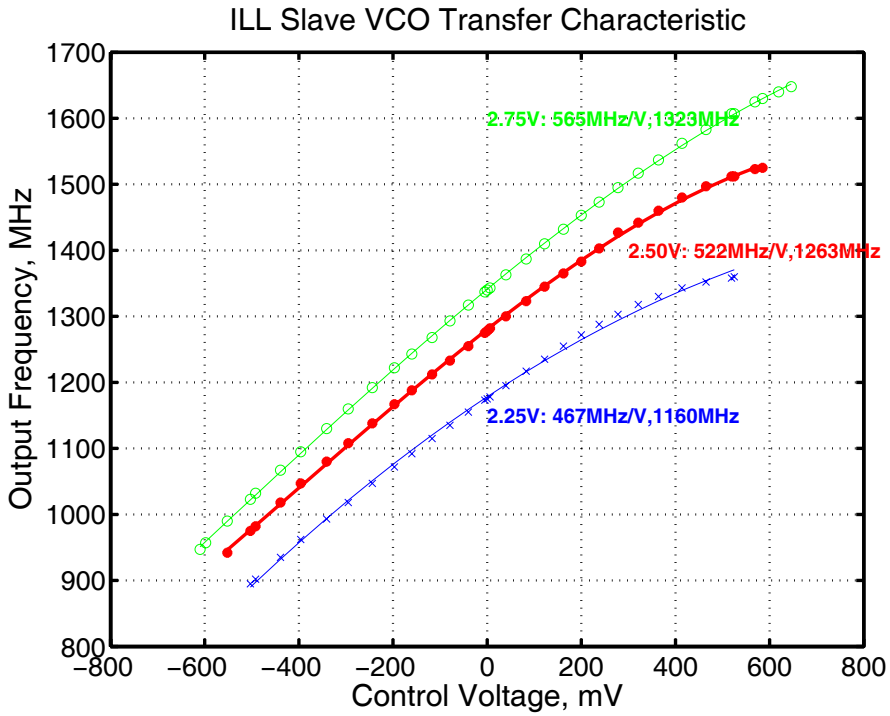

Figure 5-23 ILL slave VCO transfer characteristic

led to its discovery and modeling.

There remains a significant task in performing more experiments to validate and fully characterize the behavior of the injection-locked loop. In the current implementation, when injection is enabled, the locking range is smaller than expected. The loop also hads a large offset due to a layout error causing it to drift all the way up to the power supply rail.

5.9 Appendix: A Simple PLL Design Recipe

In this section we present a simple design recipe for a third order, type-II phase-locked loop as shown in Figure 5-24(a). A PLL is composed of a voltage-controlled oscillator (VCO), frequency divider (FD), and a phase frequency detector (PFD) in a feedback loop. The VCO's frequency is scaled by the FD so that it can be compared by the phase detector with a very precise reference frequency. In essence, the VCO frequency tracks the frequency of the reference, but at a multiple of the frequency divider ratio. So, for example, if the reference is oscillating at 10 MHz and the FD is set to divide by 100, the VCO frequency becomes 1000 MHz.

The phase-frequency detector used in this example is the well-known topology shown in Figure 5-25. This is a standard latch-based design, where all signal paths have been equalized to minimize reference spurs. The output signals *up*, *dn* and their complements have pulse widths that are proportional to the phase difference between the *r* and *v* inputs.

The charge pump is also of conventional design (Figure 5-26). The I_{UP} and I_{DN} currents are generated by matched NMOS cascoded mirrors also to minimize spurs. PMOS dummy switches are used to reduce errors due to charge injection (**MP1**). The output stage is a folded cascode using wide-swing cascoded mirrors for low voltage operation.

.The combination of charge pump and loop filter realizes a series phase-lead controller. The controller adds a pole and a zero to the open loop transfer function. One pole, T_P, is at the origin. An extra pole due to C_1 mitigates the reference spurs due to charge pump mismatch and leakage by filtering the high frequency ripple in V_{CTL}. The impedance *Z(s)* of the second order passive filter

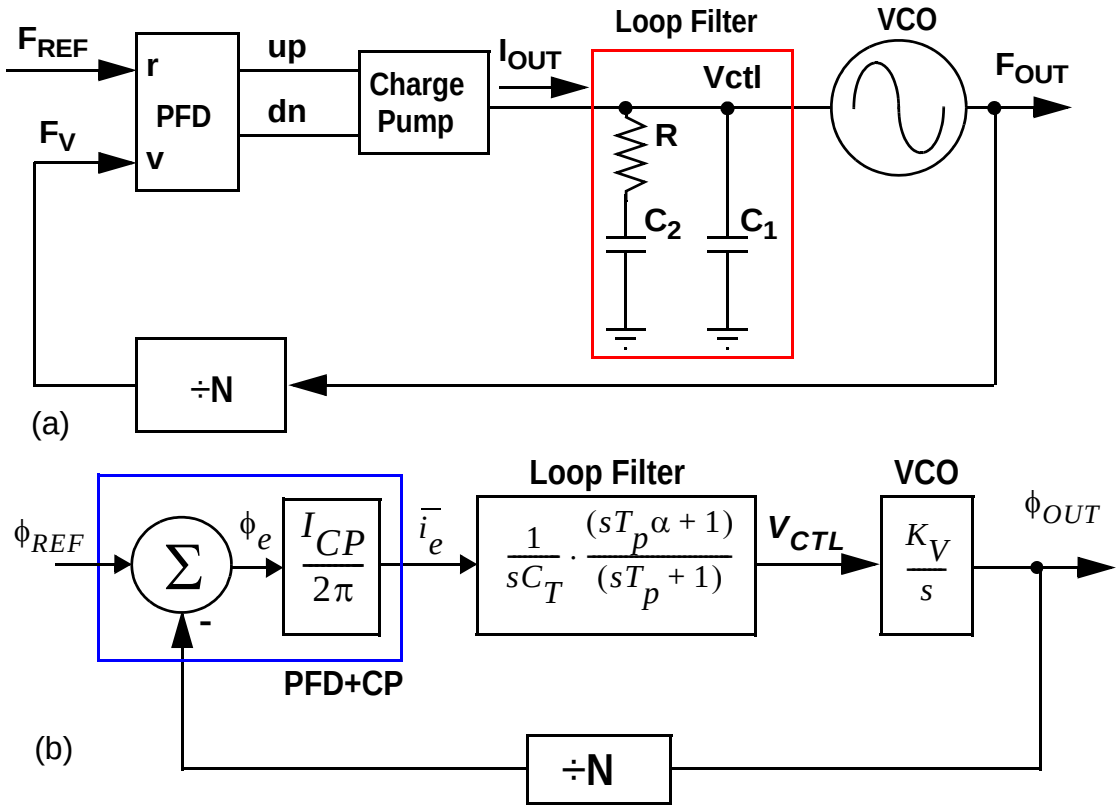

Figure 5-24 Third order phase-locked loop: (a) Block diagram; (b) Linearized model

converts the charge pump output current into the VCO control voltage, Vctl, as shown in:

$$Z(s) = \frac{1}{sC_T} \cdot \frac{(sT_p\alpha + 1)}{(sT_p + 1)}, \tag{5-11}$$

$$C_T = C_1 + C_2, \tag{5-12}$$

$$T_p = R \cdot (C_1 \| C_2), \tag{5-13}$$

$$\text{and } T_p\alpha = R \cdot C_2, \tag{5-14}$$

where T_P and αT_P are the pole and zero introduced by the loop filter, respectively.

Figure 5-24(b) shows the linearized model for the PLL. The open loop transfer function *L(s)* of this system is given by:

$$L(s) = \frac{I_{CP} \cdot K_V}{2\pi \cdot C_T \cdot N} \cdot \frac{(sT_p\alpha + 1)}{s^2(sT_p + 1)}, \alpha > 1, \tag{5-15}$$

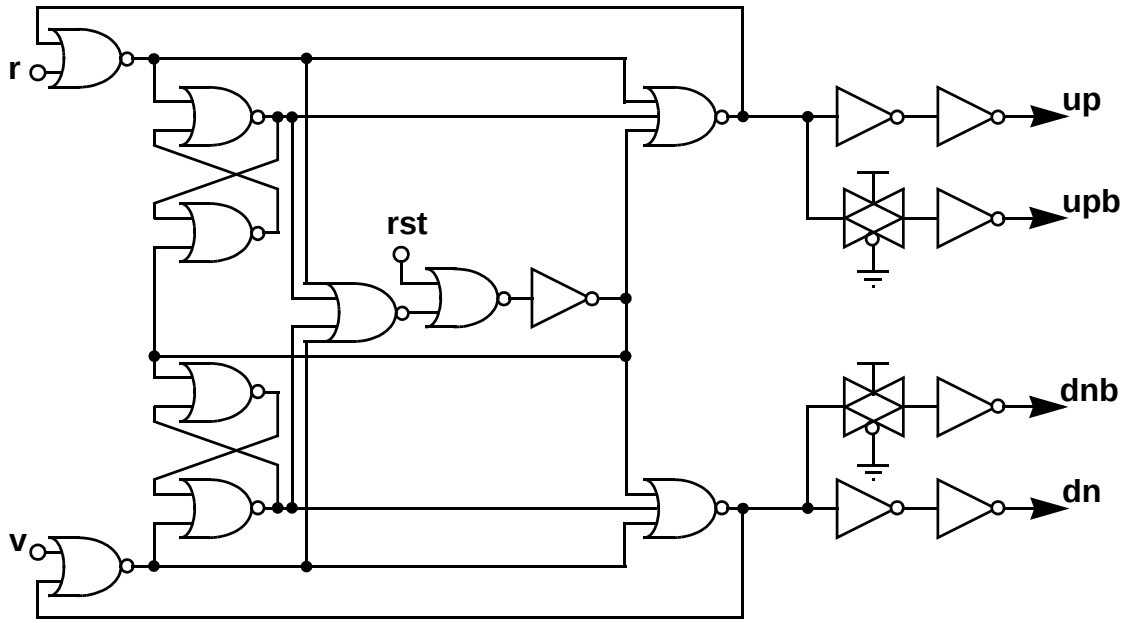

Figure 5-25 Phase-frequency detector

where I_{CP} is the nominal charge pump current, K_V is the gain of the VCO, N is the frequency division ratio of the feedback path, C_T is the total capacitance of the loop filter, T_P is the pole introduced by the loop filter, and α is the pole-zero ratio. Because of the two integrators, the system is type-II, which means that there is zero steady-state phase error for a frequency step[7].

We can observe from the root locus of *L(s)* (Figure 5-27) that the loop is always stable at all gains, for reasonable values of α. The encircling of the zero by the closed-loop poles reduces sensitivity of the PLL to gain variations.

For the controller used, the maximum phase lead occurs at the geometric mean of the pole and zero locations (Equation 5-15) [Kuo82]. We want to place this phase lead at the loop crossover frequency F_C for maximum phase margin, ϕ_M, and minimum locking time [Banerjee03]. Using Equations 5-11 and 5-15

7. A frequency step is equivalent to a phase ramp.

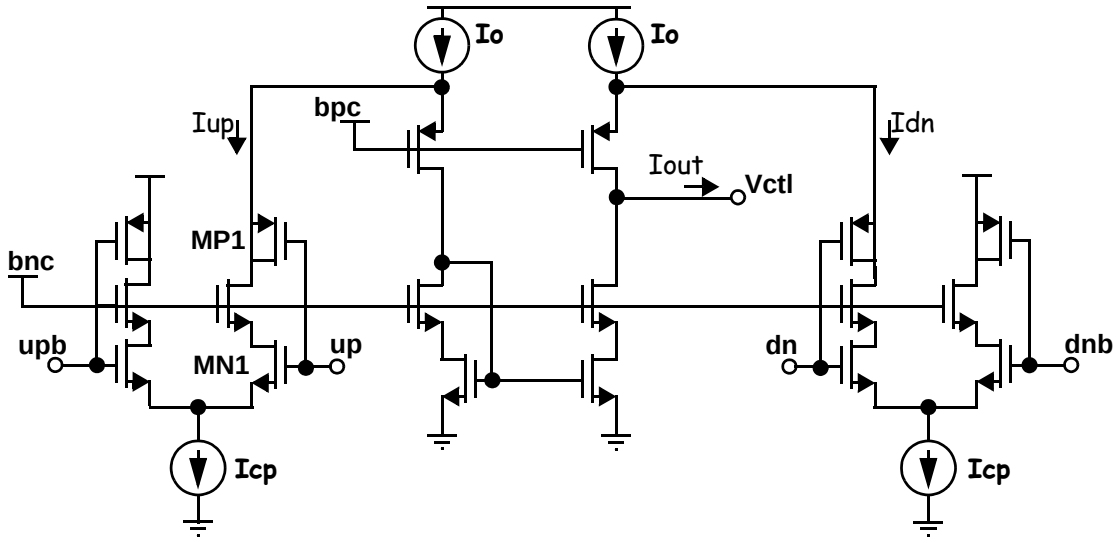

Figure 5-26 Charge pump

we can derive an expression for phase margin ϕ_M:

$$\omega_M = \frac{1}{T_p\sqrt{\alpha}}, \tag{5-15}$$

$$\phi_M = \text{asin}\left(\frac{\alpha - 1}{\alpha + 1}\right), \tag{5-16}$$

$$\alpha = \beta + 1, \tag{5-17}$$

$$\text{and } \phi_M = \text{asin}\left(\frac{\beta}{\beta + 2}\right), \tag{5-18}$$

$$\text{where } \beta = C_1 / C_2 . \tag{5-19}$$

According to these expressions, the phase margin becomes a function of pole/zero ratio, α, which is a function of capacitor ratio β. This property is very useful, as it means that the phase margin is not sensitive to variations in the resistor value, but only to the capacitor ratio, which is much more easily controlled by proper layout techniques. Figure 5-28 plots Equation 5-18, and shows the phase margin as a function of capacitor ratio. We observe that, for a phase margin of 52°, the required capacitor ratio β is 8, which is very convenient for layout.

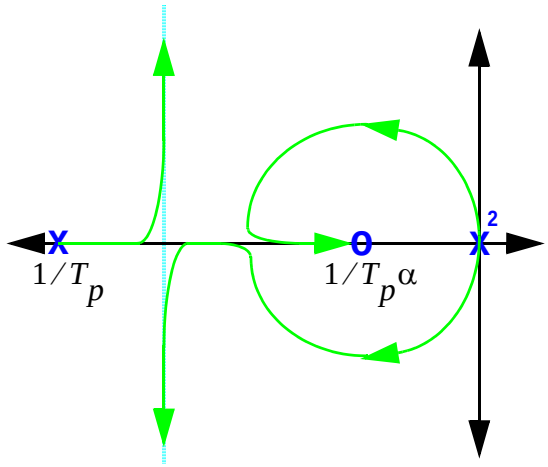

Figure 5-27 Root locus for third order phase-locked loop

To minimize capacitance mismatch we may use a common-centroid configuration using a 3x3 array of square-shaped unit capacitors of value C2, where C1 is comprised of the 8 units along the periphery of the array. For even better matching the capacitor array should be surrounded by dummy capacitors.

Finally, we present a design example. Assume a PLL with output frequency F_{OUT} of 1GHz and reference F_{REF} = 62.5MHz. This leads to N = 16. Let's further assume that the open loop unity gain bandwidth F_C is set at 2MHz and that we want to compensate the loop to achieve a phase margin ϕ_M of 53°. To minimize power dissipation, we select a charge pump current I_{CP} of 10 μA. The gain of the VCO, K_V, is determined from circuit simulations to be 465 MHz/V at the slow corner[8]. Selecting β = 8 for phase margin of 53° leads to the following values for the filter components: C1 = 4.9pF, C2 = 614fF, and R2 = 48.6kΩ. A plot for the simulated startup behavior of the PLL is shown in Figure 5-29. Further analysis using the system's root locus, shows that the phase

8. Using the circuit from Figure 5-11.

margin degrades by only 4° for a variation in the open loop gain of a factor of four (i.e., gain varies from 0.5 to 2.0 of nominal value).

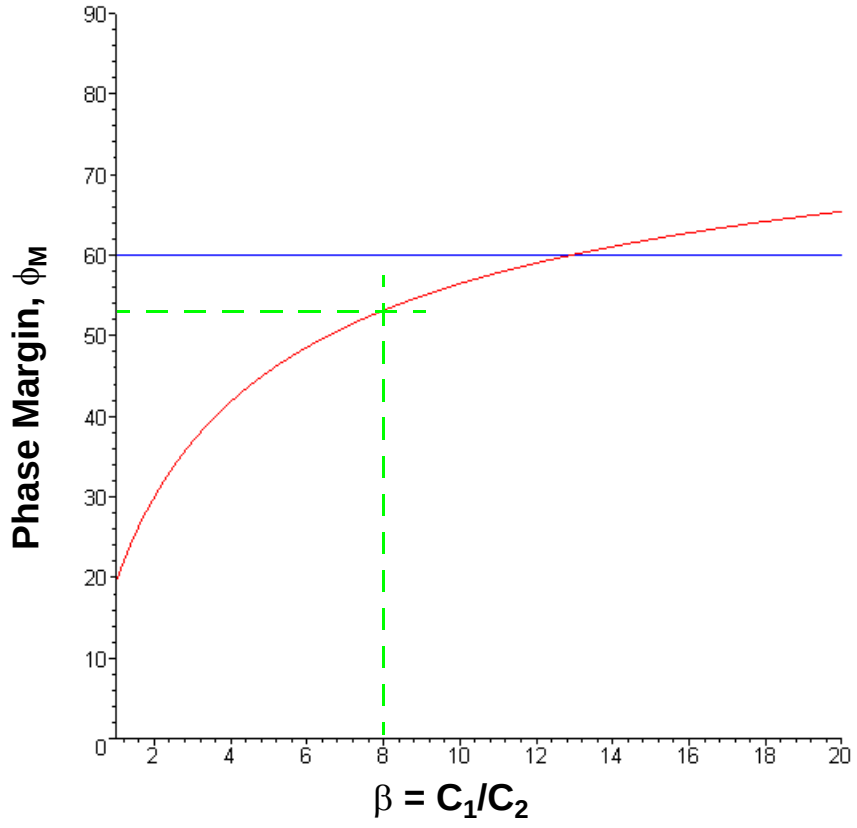

Figure 5-28 Phase margin vs. filter capacitor ratio for third-order phase-locked loop

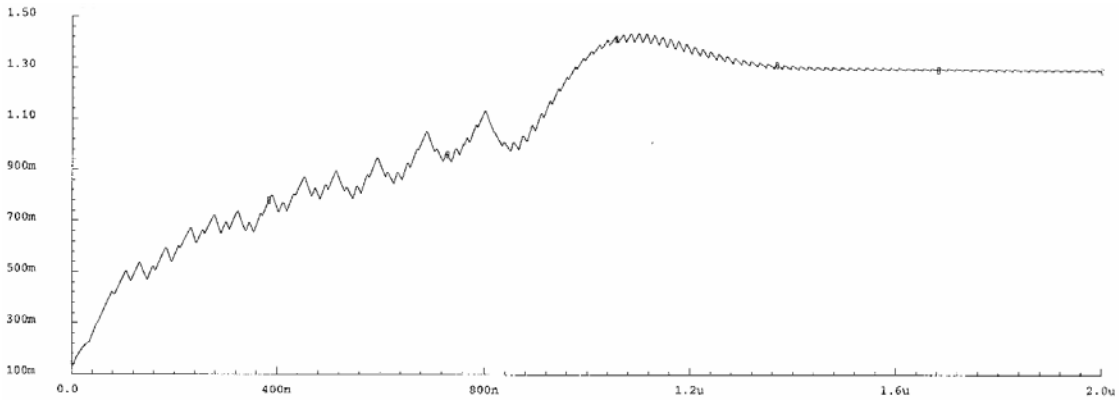

Figure 5-29 Example PLL startup transient

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Chapter 6

Conclusions

In this work, we have described design techniques for low-power, communications-grade integrated VCOs and frequency dividers in CMOS technology.

First, we proposed a methodology that uses a new phase noise model to trade-off phase noise and power dissipation in the design of ring oscillators. We discussed the design of low-power differential CMOS ring oscillators suitable for RFIC frequency synthesis and carried out experiments to evaluate different ring oscillator topologies along the noise vs. power design envelope. Furthermore, we tested three different topologies of ring oscillators, including a cross-coupled topology that achieves lower flicker noise upconversion by exploiting waveform symmetry.

Second, we studied the injection-locking mechanism and how it can be exploited to achieve low-power frequency division using CMOS ring oscillators. We presented experimental results to validate our model and proved that injection-locked differential CMOS ring oscillator frequency dividers operate at frequencies of up to 2.8 GHz with extremely high power efficiency.

Third, our experience with ring oscillator frequency dividers reveals that large modulus division comes at the expense of a very limited operating locking range. In order for the application of higher order moduli to be useful and practical, we developed a topology to extend the locking range of the injection-locked frequency divider, named the injection-locked loop (ILL). We discussed the concept of the ILL and described the evolution that led to its discovery and modeling.

Finally, we found other applications for the ILL that are described in Section 6.2.

6.1 Contributions

Much of the knowledge gained in the course of this work relates to techniques which were previously assumed to be fully explored. For instance, injection-locking was discovered long ago, but until this work, no one had used the regenerative ("Miller") divider as a model for injection-locked ring oscillators. The contributions of this thesis can be summarized as follows:

- Studied the operation of CMOS ring oscillators and phase noise performance tradeoffs using the Hajimiri linear-time-variant phase noise model.
- Described injection-locked CMOS ring oscillators using the Miller regenerative divider as a prototype for modeling the injection-lock mechanism.
- Showed the design and operation of frequency dividers that operate up to 2.8-GHz by exploiting the injection locking phenomenon in differential CMOS ring oscillators.
- Developed the injection-locked loop to extend the locking range of the injection-locked ring oscillator frequency divider.

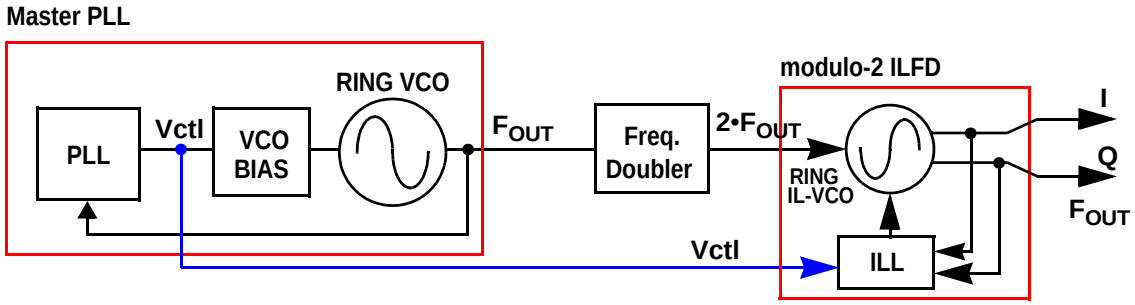

Figure 6-1 ILL-based precise quadrature generator

6.2 Recommendations for Future Exploration

There remains the significant task of performing more experiments to validate and fully characterize the behavior of the injection-locked loop. In the current implementation, the locking range is smaller than expected. The loop also has a large offset due to a layout error causing it to rail. This still needs to be fixed.

6.2.1 Precise Quadrature Generation

A possible application for the ILL is precise quadrature generation. This problem has been studied extensively. High quality precision quadrature signal sources are essential for advanced image-reject radio architectures, as well as for clock and data recovery applications. These applications have a need for wideband quadrature splitters with low phase noise. A number of quadrature generation techniques have been proposed to overcome the limitations of offsets and mismatches on the quality of quadrature signals. For instance, a flip-flop-based divide-by-two circuit triggered by a 50% duty cycle clock signal can be used to generate quadrature phases. The duty cycle dependency can be eliminated by using two dividers in series (divide-by-four), but this requires using faster technology due to the higher input frequency.

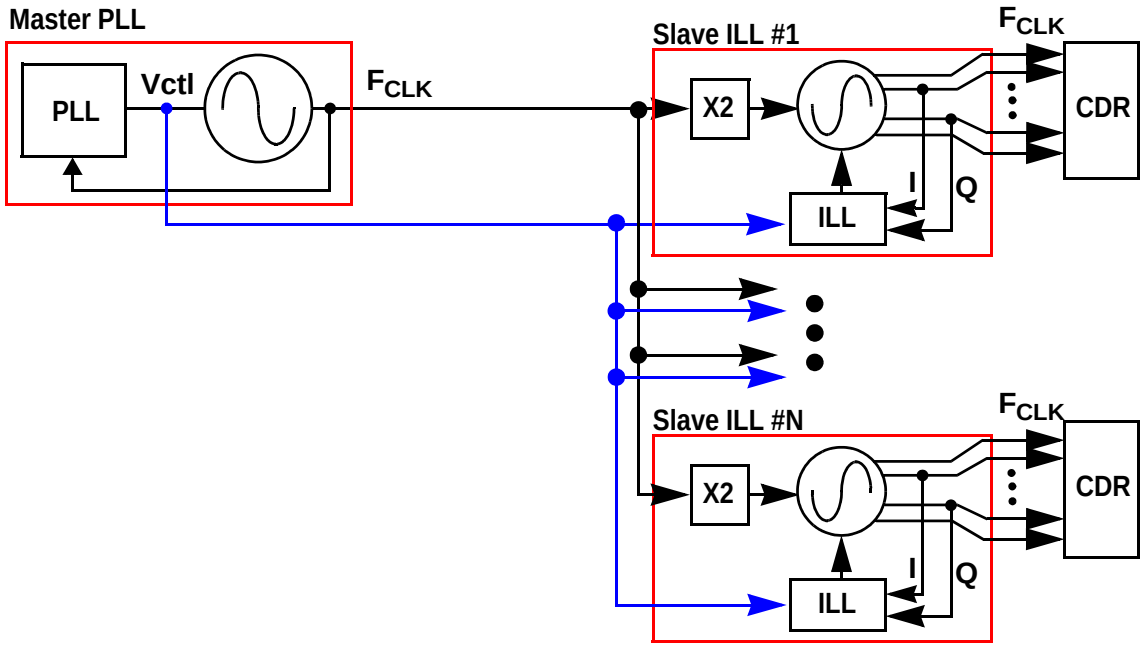

Figure 6-2 Multi-phase clock distribution using ILL

Analog techniques used vary from passive RC-CR phase splitters which are only adequate for narrowband applications [Lee98], to poly-phase filters that require large area and considerable power dissipation [Gingell73]. Another alternative is to use PLL-stabilized quadrature ring oscillators, but their quadrature accuracy is susceptible to random offsets caused by device mismatches. Kinget, et. al [Kinget02] describe a scheme that relies on the fact that quadrature outputs have less error than the inputs in an injection-locked ring oscillator. The quadrature error gets reduced for subsequent injection stages. Still, being open loop, the quadrature error is at the mercy of not only systematic and random mismatches, but also of how far the oscillator's free-running frequency is from that of the injected signal. This scheme also requires manual tuning of the oscillators.

A closed-loop approach by Navid, et. al [Navid97] uses a comparator with an adjustable threshold in front of the divide-by-two that can adjust the clock's duty cycle toward highly accurate quadrature outputs. The comparator

threshold is computed with a feedback loop which measures the quadrature error. All this technique does is eliminate the sensitivity to duty cycle variations of the digital divide-by-two circuit. It still requires an input signal at twice the output frequency.

Quadrature LC oscillators have also been used extensively, but they are sensitive to mismatches as well as quadrature offsets due to the coupling mechanism used. To correct this deficiency, Ravi, et. al [Ravi02] uses two identical anti-phase, modulo-2, LC-oscillators tuned at one half of the injected signal frequency. This scheme nulls out the error in quadrature due to injection, but cannot compensate for the effect of mismatches in the two LC oscillators.

As we know very well by now, nulling out the quadrature error is a side effect of the injection-locked loop which can also be exploited by itself. Furthermore, the ILL maximizes the noise filtering bandwidth of the oscillator, minimizing the overall phase noise and jitter due to internal noise sources. These properties make the ILL ideal for broadband quadrature generators and is an appealing solution to the quadrature offset problems faced by RFIC designers.

For instance, as shown in Figure 6-1, a master clock signal can be injected into a frequency doubler whose output is fed into a modulo-2 injection-locked 4-stage ring oscillator frequency divider (ILVCO). The ILVCO is a replica of the VCO in the master PLL, both of which operate at the same frequency. The ILVCO's natural free-running frequency can then be stabilized using the master PLL's control voltage (or a current-domain surrogate), but the frequency synchronization is achieved via the injection locking mechanism. The ILL can then correct the quadrature error of the replica ring oscillator, thus relaxing the offset and mismatch requirements of the oscillator buffer stages. In this case the ILL guarantees that the output phases are in perfect quadrature. This scheme

can even null out phase errors due to mismatches in the VCO buffer stages. Small mismatches will only make the ILL settle to a point slightly off from the free-running frequency. Furthermore, the frequency tracking behavior of the ILL tunes the ILVCO to maximize the locking range, thus minimizing the phase noise contribution of the quadrature generator.

6.2.2 Multi-phase Clock Distribution and Recovery

As the bandwidth demands of computer and digital communications systems continue to grow, high-speed serial I/O links are replacing traditional parallel buses [Farjad02]. Such high-speed I/O circuits are already found in packet switches, circuit switches, and processor-memory interconnects. Clock and data recovery (CDR) circuits for these applications usually require multiple locally-generated clock phases synchronized to a master clock. This is fertile ground for applying injection-locked techniques. For example, Lee used the filtering property of an injection-locked slave replica oscillator as a first-order low-pass filter to suppress clock jitter accumulation [MJLee03]. In this approach, the filtering bandwith is very sensitive to the injected signal amplitude, thus requiring a mechanism to stabilize the injection strength.

Another area of great interest, is the generation and distribution of accurate multi-phase clocks in systems-on-a-chip (SOC) where interconnects begin to look less like bundles of wires and more like networks [Wilson02]. The needs of on-chip interconnect begin to mimic the needs of other kinds of networks, even though the nodes and physical media are quite different. Given this problem, it is inevitable that in SoC designs, the chip becomes analogous to a single-board computer. Over the next few years, on-chip interconnect will evolve along the same lines as any other kind of network. This application is a

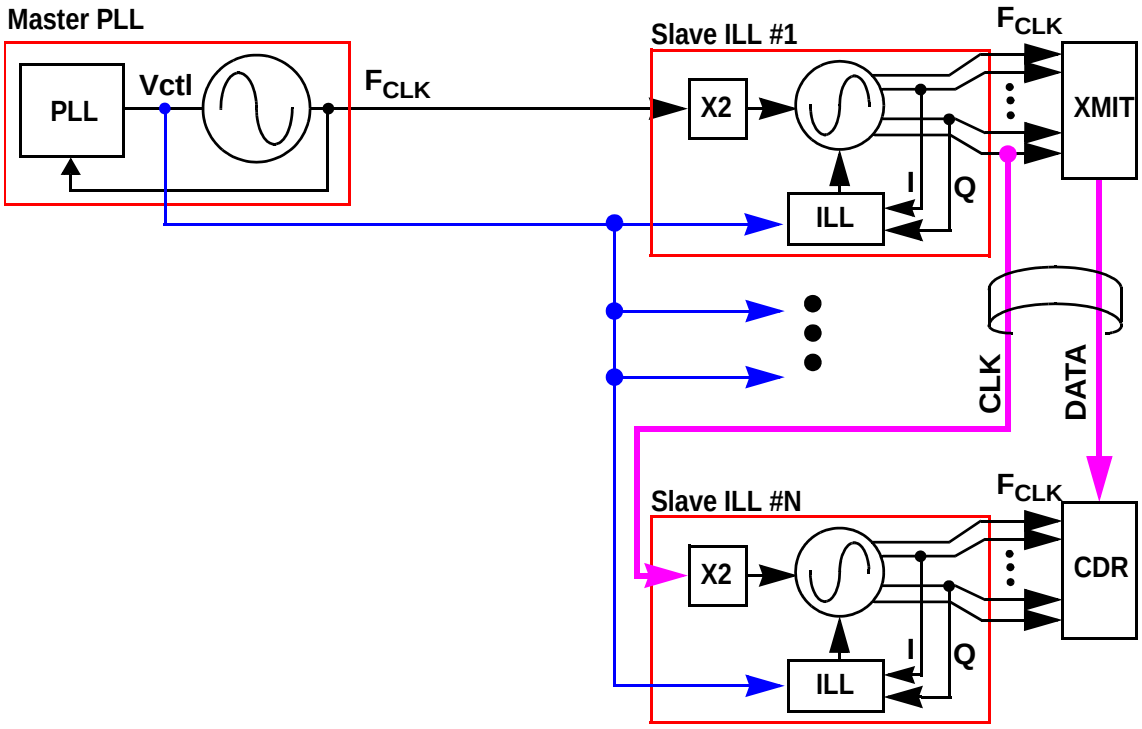

Figure 6-3 Source-synchronous clock distribution using ILL

natural fit for a simple clock distribution network based on ILL-assisted injection-locked oscillators. For example, as illustrated in Figure 6-2, injection-locked slave oscillators can be used to generate local multi-phase clock phases. The slave oscillators can be replicas of a master clock generator VCO operating at the same frequency. Injecting at the free-running frequency of the slave oscillators guarantees zero phase offset between the injected and output clocks.

Using a source synchronous technique and injecting the received clock into the ILL, we can achieve not only frequency synchronization, but phase synchronization as well (Figure 6-3). The injection mechanism ensures frequency synchronization while the ILL achieves phase synchronization by tuning the free-running frequency of the slaves to that of the received clock.

It is hoped that this thesis will enable many more applications to be found in the future for injection-locked ring oscillators.

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