RAFAEL J. BETANCOURT-ZAMORA

BETASOFT@ALUMNI.STANFORD.EDU | +1.650.224.6849 | SILICON VALLEY, CA

ENGINEERING DIRECTOR & SILICON ARCHITECT

FREQUENTLY ASKED QUESTIONS

1. Where were you previously working? What was your role?

Until recently, I was at the Mobile Silicon Division of Synaptics Inc. ("SYNA") in San Jose, California. At Synaptics, I was Director of AMS System and Verification, responsible for a global team that performs AMS system-level definition and verification of complex capacitive Touch controllers, as well as integrated Touch and LCD Display Controllers (TDDI) for mobile and automotive applications.

2. Reason for leaving or motivation in looking?

Due to a reduction in Force ("RIF") my position at SYNA was terminated on August 15, 2018.

3. What is your area of technical expertise?

My current area of expertise is Design and Verification of Analog Mixed-signal capacitive touch controllers. My current team has executed AMS verification and modeling of multiple generations of Touch/TDDI controllers. As silicon architect and design manager, not only have I defined the AMS methodology and CAD flow, I also helped defined the ISO-9000 standards for ASIC tapeout (checklists, best practices, etc.) used within the company.

Furthermore, I have been the technical/touch lead of multiple touch/TDDI controllers. In that role, I have been responsible for high-level specifications, analog micro-architecture & digital AFE control, top-level design, design reviews, pre-TO signoff, DFMEA, reference manuals & datasheets, and training in coordination with global cross-functional teams.

My research background at Stanford is Analog/RF CMOS circuits, specifically oscillator phase noise, and ultra-low-power techniques for microwave frequency dividers using injection-locking techniques for low-power frequency synthesis.

Earlier in my career I worked as Analog designer of both discrete and integrated products. I started at SYNA working on the AFE for a resistive-type sensor, and clock oscillators. Those circuits were functional in silicon, and some of them sold in the millions of units.

Pre-SYNA, I designed the analog PHY for a 480Mb/s USB transceiver in CMOS. Before that, I also designed a laptop for children (SmartPad), and a product used by orthopedic surgeons to perform precise measurements on X-rays for sizing/fitting of prostheses (X-caliper). This required interfacing MEMs accelerometers to a microcontroller.

Before that, I also designed and built instrumentation amplifiers for biopotential measurements (EEG/EMG) used for the Stanford Neural Interface and later used for a project at the School of Medicine for SIDs studies in rat models. I also worked on a Biotelemetry project for NASA, building hardware that flew on the International Space Station.

Although, I have not done hands-on transistor-level design in a while, I have kept current with my roles of touch lead and silicon architect: sign-off of block-level analog design reviews, review/assist with AMS debug pre-TO as well as during silicon bring-up, ATE test development, and assist with MP yield issues as well as field-returns/RMAs.

I am also quite familiar with intellectual property, as a reviewer of IDFs at SYNA for 10+ years, as well as having worked as an expert witness in various cases pre-SYNA.

Finally, I do have a few issued circuit patents, some of which are used in chips that have shipped millions of units: US Patent 9,778,804, US Patent 9,740,351, US Patent 8,058,884.

4. What is your ideal position and work environment?

In 2007 and 2010 I was fortunate to participate in various leadership development programs, intense experiences that shaped the kind of manager I am today. More recently, I've continued my professional development by actively participating in the Silicon Valley Chapter of the IEEE Technology and Engineering Management Society ("TEMS"), where as Vice-Chair I am responsible for educational programs for the benefit of our members: both experienced managers and those just starting out. These experiences have clearly shaped what I consider to be an optimal work environment and team.

With that said, I am primarily interested in a role where I can mentor/develop a team, while solving exciting technical challenges. That also means working smart in an honest open environment where politics are neither encouraged nor rewarded. Equally important, an optimal team is characterized by respect, conscientiousness, and recognition that a team is like a chain, which is only *"as strong as its weakest link*," and everyone is equally responsible for its strength and success.

5. Do you have experience leading new technology development? How about chip-lead experience?

For the last 15 years, I have lead multiple Touch Controller ASIC projects from concept, MRD/PRD definition, scoping, through design, tapeout, post-silicon bring-up and mass production. In all, I have worked on 30+ ASICs with billions of units shipped to date.

6. Do you have experience releasing products in high-volume?

Yes, I have released to mass production many Touch/TDDI ASICs that have shipped billions of units to date. There are ASICs released 4-5 years ago for which I still provide design expertise for Failure Analysis and Root Cause analysis of field issues, some of which are clearly beyond the 6-*sigma* design envelope.

RAFAEL J. BETANCOURT-ZAMORA

BETASOFT@ALUMNI.STANFORD.EDU | +1.650.224.6849 | SILICON VALLEY, CA

7. What is your experience of working with customers and vendors?

I have released to mass production many Touch/TDDI ASICs that have shipped billions of units to date, where I had many opportunities to interact directly with silicon foundries, service providers & contractors, CAD tool vendors, and IP vendors.

First, with foundries I had multiple times evaluated process nodes, PDKs, WAT test structures, test chips, performed cost analysis, and negotiated contracts. Second, I have specified and defined the scope of work & specifications and wrote the legal contracts for multiple external service providers and design contractors. Third, I have scoped, specified, bided-out, sourced, and negotiated contractual terms for various IPs used in SYNA ASICs.

I have also had to work closely with many customers to define the product requirements and specifications, verify the design, validate in silicon, and in multiple occasions assist with root cause analysis/FA of issues at the foundries, contract manufacturers, and field returns/RMAs. For this I have had to work extensively with the field teams and the end customers

8. What is your current location? Are you open to relocation?

I reside in Santa Clara, California. I would not consider relocation outside of the SF Bay Area at this time.

9. Are you open to travel? How about international travel?

Yes, business trips every 2-3 months are reasonable.

10. When can you start a new position?

My last day at the office will be September 17, 2018 and my last day on SYNA's payroll is November 16, 2018. I can start on December 2018 or January 2019.

11. Do you have authorization to work in the United States?

Being born in Puerto Rico, I am a U.S. Citizen by birthright without any employment restrictions. Here is my recipe for the perfect Paella. I am sure you will enjoy it!

12. How could I contribute to your company?

With my breadth of expertise in ultra-high-volume mobile/consumer electronics, extensive deep background and experience in touch sensing technology, and demonstrated leadership ability, you will not find anyone more qualified to join your team.

Timing is perfect to make this happen. What are YOU waiting for?