RAFAEL J. BETANCOURT-ZAMORA

BETASOFT@ALUMNI.STANFORD.EDU | +1.650.224.6849 | SILICON VALLEY, CA

ENGINEERING DIRECTOR & SILICON ARCHITECT

PROFESSIONAL SUMMARY

A people-oriented **Director/Architect** with 35+ tapeouts of digital/analog CMOS IC Design experience, directly responsible for the design and MP of over a billion units. Experienced in complete product lifecycle, from initial conception through design, verification, fabrication & testing. Driven by project success and the success of the team.

WORK HISTORY

2002-2018, **Synaptics, Inc.**, San Jose, CA
For this leading manufacturer of human interface sensing devices serves as follows:

Director, Analog Mixed-signal Systems and Verification (2015-2018)

- Responsible for a global team that performs AMS verification of complex capacitive Touch controllers, as well as integrated Touch and LCD Display Controllers (TDDI) for mobile and automotive applications.
- Technical lead for various TDDI controller chips that have shipped hundreds of millions of units.
- Worked with System Architects, Digital, Test, and Firmware teams to define complex interface specifications for analog touch and display control logic, and analog DFT.
- Worked closely with Apps, Firmware, and Test teams in NPI/MP of Touch and TDDI controllers. Provide technical support to field teams with RMA, and failure analysis investigations (DOE).
- Representative to the IP committee, 3 patents issued.

Principal Silicon Architect, Touch (2011-2014)

- Technical lead for Touchscreen CMOS controllers for mobile, tablet, and notebook PCs.
- Oversee silicon project definition and execution combining broad technical skills, technical lead skills and people skills to lead a talented interdisciplinary design team.

Sr. Analog Mixed-Signal Design Manager (2005-2011)

Started just after IPO ($100M revenue, $55M market cap) and managed through 30%+ year over year growth (~$2B market cap). My contributions were instrumental to the company's growth as detailed below:

- Started as manager of all ASIC Design (Digital, Analog & Mixed-signal), and grew the team up to 10 full-time IC designers. Eventually assumed management for focused Analog Mixed-signal (AMS) team.
- Managed the definition/specification for Touch sensing ASICs, working with Marketing, Apps, FW and other internal customers: silicon roadmap (MRD/PRD), technology scoping and feasibility studies.
- Managed contractors (NDA, negotiated contracts, managed progress). Negotiated with third-party IP vendors as well as silicon foundries.

Senior Analog IC Design Engineer (2003-2005)

- Designed analog circuits for low-power, low-cost capacitive & resistive sensing ASICs.
- Technical lead for various Touch Controller ASICs, responsible for project management: supervised and mentored junior designers and layout/mask design contractors.

Senior Analog IC Design Contractor (2002-2003)

- Designed analog circuits for low-power, low-cost capacitive and resistive sensing ASICs.

Innovative Semiconductors, Inc., Mountain View, CA. **Sr. Mixed-signal IC Design Engineer (1998-2001)**

- **USB 2.0:** Designed 480Mb/s analog PHY for USB 2.0 in *0.25um and 0.18um* CMOS processes.
- **IEEE-1394:** analog verification of 400Mb/s PHY, bench testing & characterization in *0.35um & 0.18um* CMOS.

Hughes Aircraft Company, El Segundo, CA. **Member of the Technical Staff, MTS-I.**

- Design & verification of a 5.2K-gates 160MHz FIR image processing chip using GaAs HEMT.

RAFAEL J. BETANCOURT-ZAMORA

BETASOFT@ALUMNI.STANFORD.EDU | +1.650.224.6849 | SILICON VALLEY, CA

EDUCATION

Engineers Degree in Electrical Engineering (D. Eng.), **Stanford University**, Stanford, CA.
Emphasis in Circuits, Analog Instrumentation, Architecture, VLSI & low-power CMOS radio frequency circuits.
Additional courses in Engineering Management, Entrepreneurship, and Intellectual Property Law.

- **Thesis:** *Injection-locked ring oscillator frequency dividers*. Advisor: Thomas H. Lee

MSEE, **University of Southern California**, Los Angeles, CA.

- Specialized in analog and digital IC design.

BSEE, **University of Puerto Rico**, Mayagüez, Puerto Rico.

- Completed a 5-year program in 4 years. Graduated *magna cum laude* with a specialization in electronics.

SELECTED CONSULTING EXPERIENCE

Pennie & Edmonds, LLP, Palo Alto, CA. **IC Design Consultant.**
Analyzed technical patents for infringement, reviewed technical documents to explain operation of complex digital ICs. Worked with attorneys to prepare for patent application filing and infringement litigation.
Eisenlohr Technologies, Inc., Davis, CA. **Hardware Design Consultant for X-Caliper Project.**
Product development and design the hardware for X-Caliper, a portable battery-operated instrument used to perform precise measurements of dimensions and angles on X-ray films using MEMs inclinometers.
Jefferson Laboratories, Inc., Palo Alto, CA. **RF Engineer.**
Performed experimental research in antennas for biotelemetry under a NASA contract for the Rodent Advanced Flight Habitat (RAHF) flown in the Space Shuttle in May 1998.

SELECTED INTERNSHIPS

Sun Microsystems Inc., Sunnyvale, CA. **Architecture Verification Engineer.**
Verified the architecture of the UltraSPARC V.9 64-bit superscalar processor.
Silicon Graphics Inc., Mountain View, CA**. Digital Verification Engineer.**
Verified functionality of a high-performance 80K-gates I/O-DMA controller for R4400 Onyx graphics workstation.
Intel Corp., Santa Clara, CA. **Micro-architecture Verification Engineer.**
Verified the architecture of the Pentium processor using an FPGA Rapid Prototyping System that ran successfully DOS, Windows, UNIX and various applications in a PC environment.

SELECTED CONTINUING EDUCATION

- **Synaptics Leadership Development Forum**, 2010.
- **Kepner-Tregoe Decision Analysis,** Santa Clara, 2008.
- **Leadership Development Program, Center for Creative Leadership**, San Diego, August 2007.
- **RF IC Design for Wireless Communication Systems, MEAD Micro.**, San Francisco, 1996.

SELECTED PUBLICATIONS

- **"Calibrating Charge Mismatch in a Baseline Correction Circuit,"** US Patent 9,778,804, (issued October 3, 2017).
- **"Multi-Step Incremental Switching Scheme,"** US Patent 9,740,351, (issued August 22, 2017).
- **"System and method for measuring a capacitance and selectively activating an indicating transducer,"** US Patent 8,058,884, (issued November 15, 2011).
- **1-GHz and 2.8-GHz CMOS Injection-locked Ring Oscillator Prescalers,** *VLSI Symp. 2001*, Kyoto.

PROFESSIONAL MEMBERSHIPS & AFFILIATIONS

IEEE Senior Member, 2018 Vice-Chair of Silicon Valley Chapter of the Technology and Engineering Management Society), member SSC & CAS Societies (Reviewer for TCAS-I and TCAS-II Journals); Tau Beta Pi; Phi Kappa Phi