RAFAEL J. BETANCOURT-ZAMORA

BETASOFT@ALUMNI.STANFORD.EDU | +1.650.224.6849 | SILICON VALLEY

ENGINEERING DIRECTOR | SILICON ARCHITECT | AMS METHODOLOGY EXPERT

PROFESSIONAL SUMMARY

Director/Architect with 35+ tapeouts of analog/digital mixed-signal CMOS IC Design experience, directly responsible for the design and MP of over a billion units. Experienced in complete product lifecycle, from initial conception through design, verification, fabrication & testing. Driven by project success and the success of the team.

WORK HISTORY

2002-2018: ***Synaptics, Inc.,*** San Jose, CA – a leading manufacturer of human interface sensing devices.

Director, Analog Mixed-signal Systems and Verification (last 4 years)

Started just after IPO ($100M revenue, $55M market cap) and managed through 30%+ year over year growth ($1.8B market cap). Responsible for a global team that performs AMS verification of complex capacitive Touch controllers, as well as integrated Touch and LCD Display Controllers (TDDI) for mobile and automotive applications.

- As technical lead for various Discrete/TDDI touch controller chips that have shipped hundreds of millions of units, managed the definition/specification for Touch sensing ASICs: silicon roadmap (MRD/PRD), technology scoping and feasibility studies.
- Established Analog Mixed-signal simulation and flow in SYNA and created a "special forces" AMS elite team trained in AMS debug, verification, and modeling. Evangelized and implemented best practices include Verilog-AMS modeling for functional verification, and the use of SystemVerilog extensions to model voltage/current & charge flow in analog behavioral models running in the digital event-driven simulator (NCSIM, VCS). Collaborated extensively with digital team to integrate SV-based AMS simulations in UVM self-checking environment. Implemented flow in 3 tapeouts and found functional bugs missed by digital DV in one ASIC pre-metal release.
- Championed AMS flow via cross-functional collaboration and AMS forum for sharing of best practices across the company (via SYNA R&D Conferences, and AMSCON-2017). Defined disruptive silicon strategy for ASIC team.
- Defined the ISO-9000 ASIC quality process, authored/edited reference manuals and users' guide as well as other documentation for Touch controllers. Provided training to global Firmware, Test, and Applications teams.
- Worked with System Architects, Digital, Test, and Firmware teams to define complex interface specifications for analog touch and display control logic, and analog DFT.
- Managed contractors (NDAs, negotiated contracts, managed progress) and evaluated/negotiated with third-party IP vendors as well as silicon foundries.
- Worked closely with Apps, Firmware, and Test teams in NPI/MP of Touch and TDDI controllers. Provide technical support to field teams with RMA, and failure analysis investigations (DOE/DFMEA).
- Evaluated 1000s of Invention Disclosures (IDFs) over 14+ years as ASIC representative to the corporate IP committee. Helped defined the corporate IDF process/strategy and helped interview/hire IP engineers, agents, and attorneys. Experienced in IP litigation as subject matter expert (deposed by opposing Counsel and testified in Federal Court). Inventor or co-inventor in 3 issued patents.

Principal Silicon Architect, Touch – Technical lead for Touchscreen CMOS controllers for mobile, tablet, and notebook PCs. Oversee silicon project definition and execution combining broad technical skills, technical lead skills and people skills to lead a talented interdisciplinary design team.

Sr. Analog Mixed-Signal Design Manager – Managed all ASIC Design (Digital, Analog & Mixed-signal), and grew the team up to 10 full-time IC designers. Assumed management for focused Analog Mixed-signal (AMS) team.

Senior Analog IC Design Engineer – Technical lead for various Touch Controller ASICs, responsible for project management: supervised and mentored junior designers and layout/mask design contractors. Designed analog circuits for low-power, low-cost capacitive & resistive sensing ASICs.

Senior Analog IC Design Contractor – Designed analog circuits for low-power, low-cost capacitive and resistive sensing ASICs.

1998-2001: ***Innovative Semiconductors, Inc.,*** Mountain View, CA. – **Sr. Mixed-signal IC Design Engineer**

Designed USB-2.0 480Mb/s PHY; Verified, tested, and characterized IEEE-1394, 400Mb/s PHY.

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EDUCATION

Engineers Degree in Electrical Engineering (D. Eng.), **Stanford University**, Stanford, CA.

- Specialized in VLSI, Analog Mixed-signal & low-power CMOS RF circuits, analog instrumentation, digital architecture. Courses in Engineering Management, Entrepreneurship, and Intellectual Property Law.
- **Thesis:** *Injection-locked ring oscillator frequency dividers*. Advisor: Thomas H. Lee

MSEE, **University of Southern California**, Los Angeles, CA.

- Specialized in analog and digital IC design.

BSEE, University of Puerto Rico, Mayagüez, Puerto Rico.

- Completed a 5-year program in 4 years. Graduated *magna cum laude* with a specialization in electronics.

SELECTED PUBLICATIONS

- **"Calibrating Charge Mismatch in a Baseline Correction Circuit,"** US Patent 9,778,804, issued October 3, 2017.
- **"Multi-Step Incremental Switching Scheme,"** US Patent 9,740,351, issued August 22, 2017.
- **"System and method for measuring a capacitance and selectively activating an indicating transducer,"** US Patent 8,058,884, issued November 15, 2011.
- **1-GHz and 2.8-GHz CMOS Injection-locked Ring Oscillator Prescalers,** *VLSI Symposium. 2001*, Kyoto.

SELECTED PROFESSIONAL DEVELOPMENT

- **Synaptics Leadership Development Forum**, Los Gatos, CA.
- **Kepner-Tregoe Decision Analysis Workshop,** Santa Clara, CA.
- **Leadership Development Program, Center for Creative Leadership**, San Diego, CA.
- **RF IC Design for Wireless Communication Systems, MEAD Micro.**, San Francisco, CA.

SELECTED CONSULTING EXPERIENCE

- **Pennie & Edmonds, LLP**, Palo Alto, CA. **IC Design Consultant –** Analyzed technical patents for infringement, reviewed technical documents to explain operation of complex digital ICs. Worked with attorneys in patent application filing and infringement litigation.
- **Eisenlohr Technologies, Inc.**, Davis, CA. **Hardware Design Consultant, X-Caliper Project** – Product development and design the hardware for X-Caliper, a portable battery-operated instrument used to perform precise measurements of dimensions and angles on X-ray films using MEMs inclinometers.
- **Jefferson Laboratories, Inc.**, Palo Alto, CA. **RF Engineer** – Designed experimental antennas for biotelemetry under a NASA contract for the Rodent Advanced Flight Habitat (RAHF) flown in the Space Shuttle in 1998.

SELECTED INTERNSHIPS

- **Sun Microsystems Inc.**, Sunnyvale, CA. **Architecture Verification Engineer –** Verified the architecture of the UltraSPARC V.9 64-bit superscalar processor.
- **Silicon Graphics Inc.,** Mountain View, CA**. Digital Verification Engineer –** Verified functionality of a high-performance 80K-gates I/O-DMA controller for R4400 Onyx graphics workstation.
- **Intel Corp.**, Santa Clara, CA. **Micro-architecture Verification Engineer –** Verified the architecture of the Pentium processor using an FPGA Rapid Prototyping System that ran successfully Windows, UNIX and various graphics applications in a PC environment.

PROFESSIONAL MEMBERSHIPS & AFFILIATIONS

IEEE Senior Member & 2018 Vice-Chair of Silicon Valley Chapter of the Technology and Engineering Management Society (reviewer for TEMSCON), member Solid-State Circuits & Circuits & Systems societies (reviewer for ISCAS, TCAS-I and TCAS-II Journals); Volunteer at IEEE Global Humanitarian Technology Conference 2018; Volunteer Judge at International Science & Engineering Fair (ISEF), 6 times; member of Tau Beta Pi & Phi Kappa Phi honor societies.